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# Volari™ V3XE Databook

## Revision History:

### Revision V1.0 (April 19, 2006)
- Change the V3XE AGP capability from 8X to 4X.

### Revision V0.94 (February 23, 2006)
- Modify the information of Video Bridge support

### Revision V0.93 (February 17, 2006)
- Modify the information of SiS302LV/SiS302ELV support

### Revision V0.9 (December 23, 2005)
- First preliminary release

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# 1 Volari™ V3XE 256-bit GPU

## 1.1 Introduction

Volari™ V3XE GPU is the affordable 3D programmable graphics processor of the XGI™ Technology 256-bit GPU family in mainstream market. With a 812-ball 31mmx31mm PBGA package, Volari™ V3XE integrates an 4X/2X AGP controller with full side-band or pipeline support, a 256-bit 3D/2D graphics engine and a motion compensation MPEG I/MPEG II accelerator. It offers a complete 64-bit DDR memory data bus. Embedded with a 256-bit 2D engine, it could achieve ultra high 2D performance with the maximum memory bandwidth up to 3.2 GB/s(DDR @200MHz). An optimized 3D pipeline architecture is implemented for eliminating the overhead resulted from texture read, Z-buffer read/write and destination read latencies and achieving a sustain throughput of over 90% of peak throughput when texture, Z buffer and alpha blending functions are all enabled. Volari™ V3XE GPU also includes a video accelerator and high performance DVD/HDTV motion compensation logic to provide very smooth DVD/HDTV playback. Volari™ V3XE GPU provides dual 12-bit DDR (dual data rate) digital interface to support secondary display, which is independent of primary CRT display.

301, which is an accompany chip of XGI™ Technology VGA chip:

- A NTSC/PAL video encoder with Macrovision™ Ver.7.1.L1 option for TV display.
- HDTV video encoder, which supports 480i, 480p, 1080i, and 720p output modes.
- A single link TMDS transmitter with excellent scaling capability for TFT LCD panel display.
- An analog RGB to support a secondary CRT monitor display.

All the above functions could support dual-display features. It means that the second display device driven by 301 could display independent resolutions, color depths and frame rates different from the traditional CRT monitor driven by primary VGA chip. 301 receives digital video signals and control signals from the primary VGA chip then transforms them into composite, S or component video outputs for TV display, TMDS signals for LCD display. The output display combination could be one of the three:

(1) Primary CRT+301-TV,
(2) Primary CRT+301-LCD
(3) Primary CRT+301-CRT.

The package type of 301 is 128-pin TQFP.

SIS302LV/SiS302ELV, which is an accompany chip of XGI™ Technology VGA chip:

- A NTSC/PAL video encoder with Macrovision™ Ver.7.1.L1 option for TV display. (For SiS302LV only)
- A dual link LVDS transmitter with bi-linear scaling capability for TFT LCD panel display.

All the above functions could support dual-display features. It means that the second display device driven by SIS302LV/302ELV could display independent resolutions, color depths and frame rates different from the traditional CRT monitor driven by primary VGA chip. SIS302LV/302ELV receives digital video signals and control signals from the primary VGA chip then transforms them into composite, S or component video outputs for TV display (For 302LV only), LVDS signals for LCD display. The output display combination could be one of the three:

(1) Primary CRT+SIS302LV-TV,
(2) Primary CRT+SIS302LV/302ELV-LCD
(3) SiS302LV-TV + SIS302LV-LCD.

The package type of SIS302LV or SiS302ELV is 128-pin LQFP.

## 1.2 Volari™ V3XE GPU Features

**PCI Bus Interface**

- Supports 32-bit PCI local bus standard Revision 2.2 compliant
- Supports 66Mhz PCI operation
- Built-in write-once subsystem and subsystem-vendor ID configuration register for on board VGA or power on auto subsystem and subsystem-vendor ID fetching from BIOS for add-on VGA card
- Built-in PCI power management configuration register for D0, D1, D2 and D3 modes
- Supports 66 MHz zero wait-state memory mapped I/O burst write
- Built-in 66 MHz zero wait-state PCI post-write buffer with byte merge to enhance frame buffer write performance
- Built-in read cache to enhance frame buffer read performance
- Supports one-wait burst read cycle when buffer hits
- Supports automatic disconnect or retry after waiting for 16 PCI clocks when read cache misses or post write buffer is full
- Supports 4-wait signal I/O read/write cycle
- Supports full 32-bit memory frame buffer address decoding for 128MB size
- Supports full 32-bit re-locatable VGA I/O address decoding for 128 I/O ports
- Supports full 32-bit memory mapped I/O address decoding for 128KB size
- Supports full 32-bit ROM address decoding for 32KB, 64KB or 128KB size
- Supports flash memory interface for VGA BIOS
- Supports medium DEVSEL decoding timing
- Supports RAMDAC snoop
- Supports IMAC compatible PCI data format

**AGP Interface**

- Supports AGP 2.0 compliant configuration setting
- Supports AGP 4X 266 MHz with 16 stages pipeline full side-band/pipe function
- Supports AGP 3.0 compliant configuration setting
- Supports AGP 4X 266 MHz with 16 stages pipeline full side-band/pipe function
- Supports hardware auto detect for AGP1.0, AGP2.0 or AGP3.0 mode support.

**High Performance & High Quality 3D Accelerator**

- Built-in a high performance 256-bit 3D engine
  - Support 16/32 bits wide of index on vertex buffers.
  - Support 16 multi-stream sources.
  - Built-in 32-bit floating point format triangle setup engine
  - Built-in 1 set of Pixel Shader (2.0) HW capable of processing 24 bits floating point. Each set is equipped with 32 multi-threads to avoid data dependent hazard.
  - Built-in 2 pixel rendering pipelines
  - Built-in hardware stereo auto rendering engine
  - Supports AGP 4X 266 MHz for texture fetch
  - Supports AGP 4X 266 MHz for vertex fetch
  - Peak polygon rate: 50M polygon/sec @ 1 pixel/polygon with Gouraud shaded, point-sampled, linear and bilinear texture mapping
  - Peak fill rate: 500 M pixel/sec, 1000M texture/sec @ 10,000 pixel/polygon with Gouraud shaded and two bilinear textured@ 250MHz

- Built-in a high quality 3D engine
  - Support Polygon stipple.
  - Support Line width > 1
  - Support Line Pattern
  - Support Point/Line Anti-alias.
  - Fully compliant Direct3D 9.0 Vertex Shader ver. 2.0. (DirectX 9)
  - Fully compliant Direct3D 9.0 Pixel Shader ver. 2.0. (DirectX 9)
  - Support Bump Mapping, Mipmapped Cubic Mapping and Volume Texture Supports flat and Gouraud shading
  - Support Nearest, Bi-linear, Tri-linear, Anisotropic filter.
  - Support 96 bits floating point of color format in MET/MRT to preserve data precision during multi-pass.
  - Capable of processing Max. to 2 pixels with 2 textures in one clock.
  - Supports high quality dithering function
  - Supports Z-test, stencil test, Alpha-test, and scissors clipping test
  - Supports ROP
  - Supports Z-buffer, stencil buffer and alpha buffer
  - Supports 16/24 bits integer Z buffer format and 16/24/32 bits floating point Z format
  - Supports 16/32/64/128 BPP render buffer format
  - Supports 1/4/8 stencil buffer format
  - Supports 2-side stencil.
  - Supports 1/4/8 stencil buffer format
  - Supports per-pixel texture perspective correction
  - Supports 1-tap, 2-tap, 4-tap and 8-tap texture filtering
  - Supports up to 4096x4096 texture size
  - Supports rectangle structure texture
  - Supports non power of two texture size
  - Supports 8/16/24/32/64/128 bpp texture format.
  - Supports ARGB/ABGR, YUY2/AYUV, DXT1/DXT2/DXT3, U8V8/L6V5U5, R16f/R32 texture formats.
  - Supports unsigned fixed, signed fixed, floating point of texture format.
  - Supports 1/2/4 bpp palletize texture
  - Supports 16/24/32 bpp RGB/ARGB texture format
  - Supports DTX1, DTX2, DTX3 texture compression formats
  - Supports texture transparency, blending, wrapping, mirror, and clamping
  - Supports fogging, alpha blending
  - Supports vertex fogging and fog table and T/L based vertex fog range
  - Supports specular lighting
  - Supports 2X/4X full scene anti-aliasing(FSAA)
  - Supports back face culling
  - Supports auto-stereo rendering

**High Performance 2D Accelerator**

- Built-in hardware command queue
- Built-in Direct Draw Accelerator
- Built-in GDI 2000 Accelerator
- Built-in an 1T pipelined 256-bit BITBLT graphics engine with the following functions:
  - 256 raster operations
  - Rectangle fill
  - Trapezoid fill
  - Color expansion
  - Enhanced color expansion
  - Line-drawing with styled pattern
  - NT fractional point line-drawing with styled pattern
  - Multiple scan line
  - Built-in bytes pattern registers

- Built-in 8x8 mask registers
- Rectangle clipping
- Transparent BitBlt with source and destination keys
- Gradient color fill
- Anti-aliasing text drawing
- Alpha blended Bitblt
- YUV to RGB color transform Bitblt
- Source data in command queue Bitblt
- YUV420 to YUV422 format conversion Bitblt

- Supports memory-mapped, zero wait-state, burst engine write
- Built-in 64x64x2 bit-mapped mono hardware cursor
- Built-in 64x64x16 bit-mapped blended color hardware cursor
- Maximum 256MB frame buffer with linear addressing
- Supports AGP4X 266 MHz data read for all 2D engine functions
- Built-in source read-buffer to minimize engine wait-state
- Built-in destination read-buffer to minimize engine wait-state

**Complete TV-OUT Solution with 301**

- TV Display
  - Supports PAL and NTSC Systems.
  - Supports Composite, S-Video, and Component RGB (SCART) Output Signals
  - Supports Macrovision Copy Protection Process Rev. 7.1.L1
  - Supports HDTV 480i/480p/1080i/720p YPbPr Output Signals.
  - Supports Macrovision™ Copy Protection Waveforms for 480p Progressive Scan Output
  - Supports TV/Primary VGA Independent Display Resolution and Frame Rate at Enhanced mode
  - Provides Adaptive 8-Line Anti-Flicker Filtering.
  - Provides Hardware Interpolation for Programmable Under-Scan/Over-Scan Adjustment.
  - Provides Programmable Display Position Adjustment.
  - Provides Programmable Notch Filter for Cross Color Elimination.
  - Provides Chrominance Filter for Cross Luminance Elimination
  - Provides Color Saturation Adjustment for Vivid TV Output.
  - Provides Gamma Correction Independent of that of Primary VGA.
  - Auto-Sense of TV Connection

**MPEG-2 Video Decoder**

- MPEG-2 MP@ML standards compliant
- Low cost design based on MPEG-2 motion compensation layer decoding architecture Built-in motion compensation logic
- Supports either AGP bus-master or LFB-mode code fetching
- Half pixel resolution in motion compensation
- Supports up to 20 Mbit/sec bit rate decoding
- Supports VCD, DVD and HDTV decoding

**Video Accelerator**

- Supports single video windows with overlay function
- Supports YUV-to-RGB color space conversion
- Supports 4-tap video interpolation with integer increments of 1/2048
- Supports graphics and video overlay function
  - Independent graphics and video formats
  - 16 color-key and/or chroma-key operations
  - Supports YUV or RGB format chroma key
  - Rectangular video window modes
  - Video only mode
  - Video CD or DVD to HDTV playback mode
- Supports current scan line of refresh read-back
- Supports tearing free double buffer flipping

- Built-in video decoder interface
  - Conexant BT829/835 (8-bit SPI mode 1,2)
  - CCIR656 video standard(8-bit,single edge latch)
  - CCIR601 video standard(8-bit,single edge latch)
- Supports input video vertical blank or line interrupt
- Supports video capture and playback tearless auto flipping
- Supports independent VBI capture
- Supports RGB555, RGB565, YUV422, and YUV420 video capture format
- Supports RGB555, RGB565, YUV422 and YUV420 video playback format
- Supports filtered horizontal/vertical down scaling capture
- Supports filtered horizontal up and down scaling playback
- Supports mirroring capture
- Supports DVD sub-picture playback overlay
- Built-in video capture FIFO to support video capture
- Built-in independent Gamma correction RAM
- Supports horizontal/vertical cropping capture
- Supports Direct Draw Drivers

**High Efficient BroadBhan™ Memory Architecture**

- Supports DDR SDRAM type
- Supports 32MB, 64MB and 128MB memory configurations
- Supports 8Mx16, 16Mx16, 4Mx32 and 8Mx32 DDR SDRAM types.
- Supports 64-bit DDR DRAM data bus
- Supports single or dual rank configuration
- Supports internal 256-bit display memory path
- Supports VGA BIOS auto memory size detection
- Supports ping-pong banking operation by 8 bank registers

**High Integration**

- Built-in CRT FIFO to support ultra high resolution graphics modes and reduce CPU wait-state
- Built-in programmable 24-bit true-color RAMDAC up to 400 MHz pixel clock
  - Built-in reference voltage generator and monitor sense circuit
  - Supports downloadable 24 bits RAMDAC for gamma correction in high color and true color modes
  - Supports programmable 4 levels DAC current ratio
  - Supports programmable pedestal level
- Built-in three clock generators
  - Integrates PLL loop filter for CRT, DRAM and 3D Engine
- Built-in 14.318 MHz reference clock oscillator circuits
- Built-in two video line buffers for MPEG II video playback
- Built-in standard feature connector logic support
- Built-in VIP interface (no host interface)
- Built-in TV Encoder Interface
- Built-in flash ROM programming interface
- Built-in VESA Plug & Display for PanelLink Interface
- Built-in thermal diode for GPU Security

**Resolution, Color & Frame Rate**

- Supports 400 MHz pixel clock
- Supports VESA standard super high resolution graphics modes
  - 640x480 16/256/32K/64K/16M colors 85Hz NI
  - 800x600 16/256/32K/64K/16M colors 85Hz NI
  - 1024x768 256/32K/64K/16M colors 85Hz NI
  - 1280x1024 256/32K/64K/16M colors 85 Hz NI
  - 1600x1200 256/32K/64K/16M colors 85Hz NI
  - 1920x1440 256/32K/64K/16M colors 85Hz NI
  - 2048x1536 256/32K/64K/16M colors 85Hz NI
  - Low resolution modes
- Supports virtual screen up to 4096x4096

**Power Management**

- Supports power management for VGA monitor
- Supports direct I/O command to force graphics controller into standby/suspend/off state
- Power down internal SRAM in direct color mode
- Supports PCI power management configuration registers for supporting ACPI power down controller
- Power down all internal macro cells such as SRAM, DAC, clock generator, DLL when power saving mode
- Supports clock stopping for video accelerator and MPEG decoder when disabled
- Supports auto clock throttling for 2D engine, 3D engine

**Multimedia Application**

- Supports DDC1, DDC2B and DDC 3.0 specifications
- Supports RAMDAC snoop for multimedia applications

**Miscellaneous**

- Supports 32K/64K/128K Bytes ROM decoding
- Supports 20MHz SPI ROM interface
- Supports MCLK, ECLK spread spectrum for EMI
- Supports Signature Analysis for automatic testing
- Supports full scan testing
- Supports BIST for internal memory testing
- 812-balls 31mm x 31mm PBGA package

## 1.3 Single Volari™ V3XE GPU Block Diagram

**Figure 1.3-1** Volari™ V3XE GPU System Block Diagram with SiS301 Video Bridge

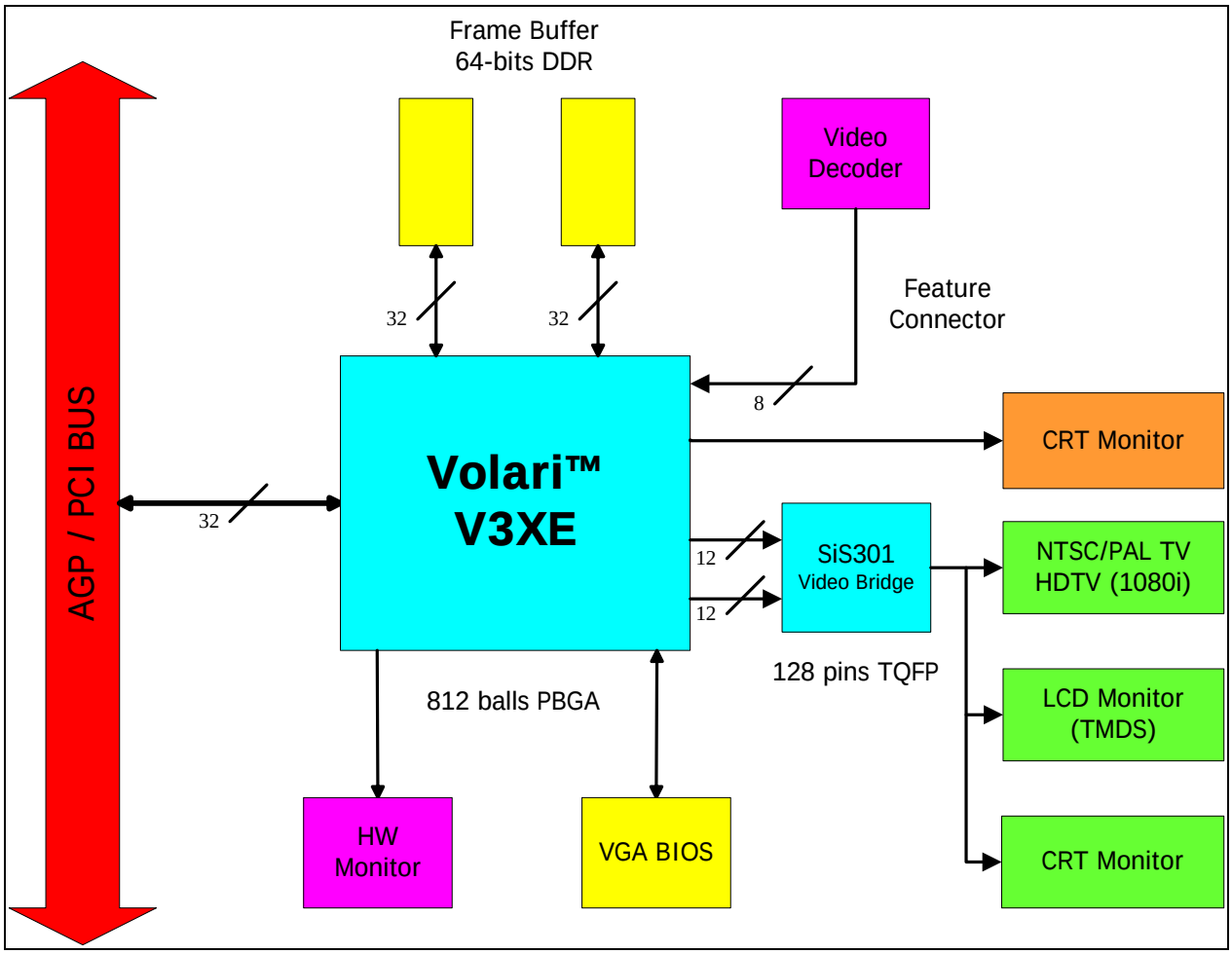


**Figure 1.3-2** Volari™ V3XE GPU System Block Diagram with SiS302 Series Video Bridge

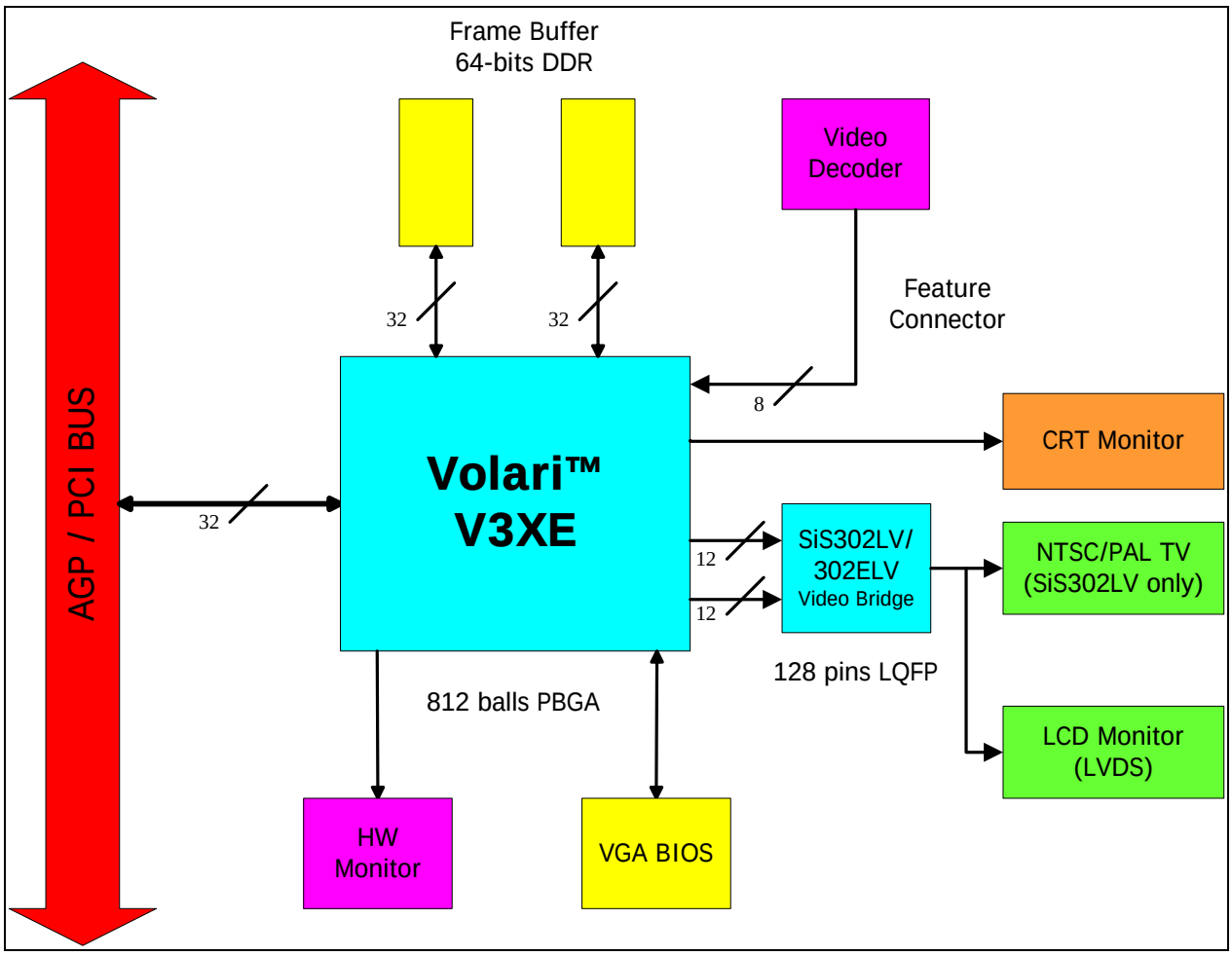
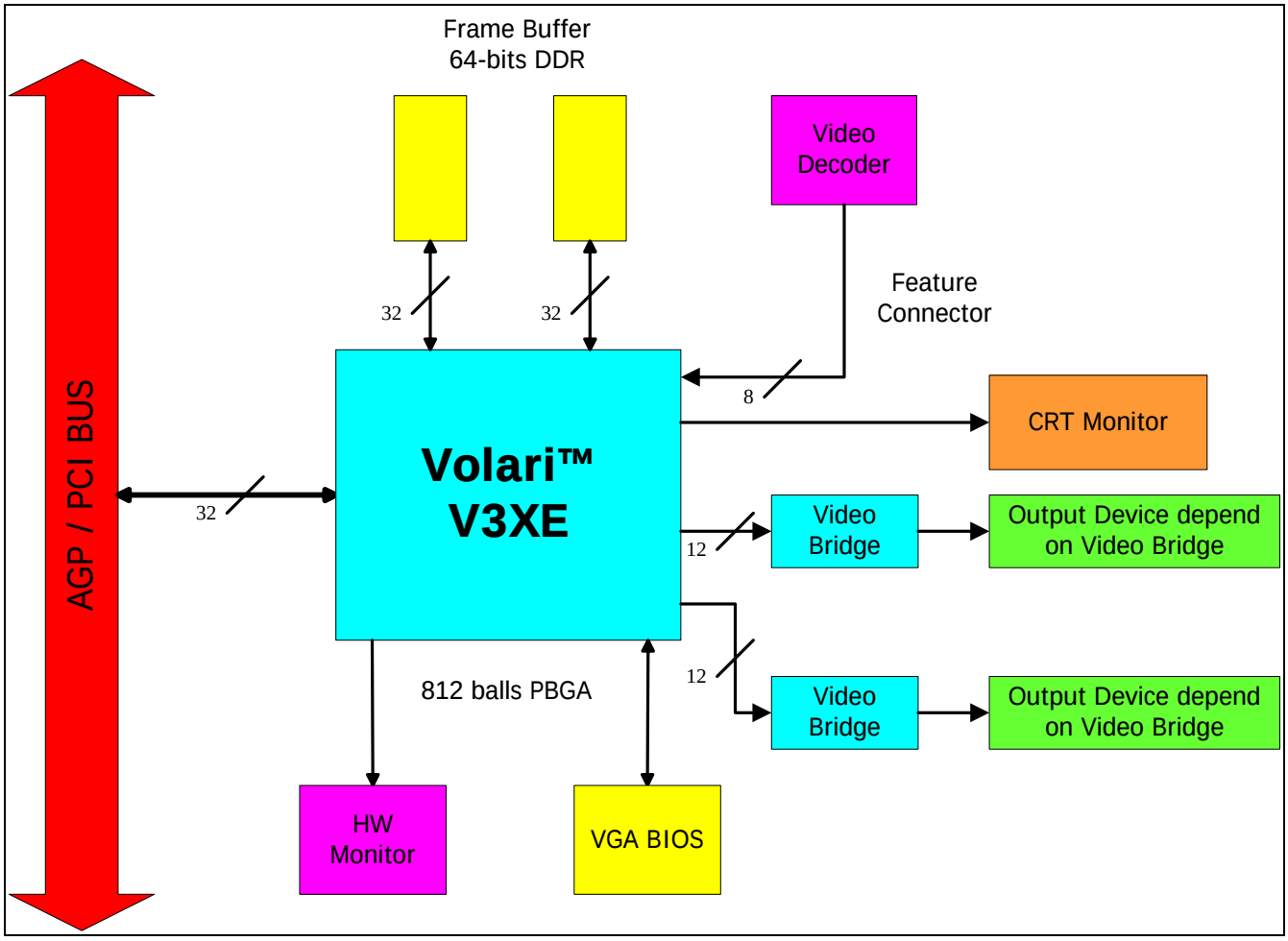


**Figure 1.3-3** Volari™ V3XE GPU System Block Diagram with Dual Video Bridges



# 2 Volari™ V3XE GPU Description

## 2.1 2D Graphics Engine

Volari™ V3XE integrated graphics controller supports a powerful graphics engine to enhance the performance. The functions of the graphics engine in Volari™ V3XE include BitBlt, Color Expansion, Enhanced Color Expansion, Line Drawing, Transparent BitBlt, Multiple Scan-line and Trapezoid Fill. The new functions of the graphics engine in Volari™ V3XE include Stretch BitBlt, Alpha blending BitBlt, Gradient fill, Anti-aliasing text.
Basically the 2D graphics engine of Volari™ V3XE GPU is a 256-bit BitBlt graphics engine. For all enhanced 256 color (8 bpp), 32k & 64k hi-color (16 bpp), 16.8 M true color (32 bpp) graphics modes, the engine supports the following functions:

- 256 raster operations
- Rectangle fill
- Trapezoid fill
- Color expansion
- Enhanced Color expansion
- Line drawing with styled pattern
- NT fractional point line drawing with styled pattern
- Multiple scan-line drawing
- Built-in 8x8 pattern registers
- Built-in 8x8 mask registers
- Rectangle Clipping
- Transparent BitBlt with source and destination ranged keys
- Source data in command queue Bitblt with small size of data

The engine also supports new GDI 2000 functions:

- Stretch BitBlt
- Gradient fill
- Alpha blending fill
- Anti-aliasing text drawing
- YUV to RGB color transform Bitblt

The following commands are specially designed for boosting the 3D and direct draw performance.

- Clear Z-buffer
- Full scene anti-aliasing Bitblt
- Video auto-flip with synchronous to 2D and 3D engines
- Capability for using AGP memory for some 2D commands

## 2.2 3D Accelerator

Targeting Microsoft Direct3D and OpenGL acceleration, Volari™ V3XE achieves extremely high fill and polygon rate in superior quality with high balanced pipeline 3D architecture. The major key technologies that guarantee a high 3D performance are the integrated Command Queue, Setup Engine, Texture Cache, and Programmable Render Engine.

The major technologies for the high performance and high quality 3D rendering in Volari™ V3XE are:

- Command Queue
- T&L Engine
- Setup Engine
- Texture Cache
- TruShaders™ Technology (includes Vertex Shader and Pixel Shader)

## 2.3 Command Queue in 3D Accelerator

Command Queue architecture wills speedup the rendering of the 3D engine. The Command Queue size is programmable from 512 KB up to 4 MB, therefore 3D driver could issue commands almost without waiting. To save the high cost for building a long hardware command queue, Volari™ V3XE could allocate a portion of the AGP memory or local video memory as the command queue buffer. When 2D or 3D engine finishes the previous command, these commands will be firstly read back as the next command for execution.

## 2.4 Setup Engine

Setup engine is one of the most critical parts in the new generation 3D architecture. It calculates and prepares all of the parameters for primitive drawing. All these computations require hundreds of addition, subtraction, multiplication, and division. If the setup calculation is executed by the host CPU, the sequential coding and processing form a bottleneck for 3D rendering.
To off-load this computation time from host CPU and to process it in parallel, Volari™ V3XE integrates a 32-bit floating point setup engine, and it could finish all of the setup computations. Furthermore, the setup engine also supports line and point setup calculations. The setup engine, specially designed to fit all the data formats in Microsoft Direct3D API, could accept vertex values directly in floating point format. One command parser is implemented for parsing vertex format into internal hardware command format for VLIW.
Once setup engine finishes the setup computations for a triangle, it transfers all these parameters to render engine within one engine clock. While rendering engine is busying drawing a triangle, setup engine could calculate the parameters needed for the next operation.

## 2.5 TruShaders™ Technology

The TruShaders™ Technology of XGI™ includes vertex shader and pixel engine.
The pixel engine is a pipelined structure engine in Volari™ V3XE GPU. It includes shading engine, pixel shader (programmable), texture engine, and post engine.
The output of shading engine is a series of pixels with color, which represents the shade of a primitive. The pixel shader, support a fully compliant DirectX 9, shader type 2.0, is programmable for additional pixel processing with plentiful and special effect, supply some microcode to CPU, it is much more flexible than legacy architecture. Texture engine is responsible for attaching the texture color on a pixel. Then, post engine will do some operations such as fogging, alpha blending, dithering and ROP for each pixel.
To support high quality texture mapping, Volari™ V3XE could support 1-tap, 2-tap, 4-tap and 8-tap texture filtering. With an integrated high-capacity texture cache, Volari™ V3XE GPU could render textures with 2 pixels per clock using 1-tap, 2-tap or 4-tap texture filtering. The video quality is normally expected to be superior for 8-tap texture mapping mode but the Volari™ V3XE GPU could support 1 pixel per clock rate when single texture map are used.

## 2.6 Texture Cache

Texture cache is a critical part of high performance 3D design. Some of the 3D chips do not have built-in texture cache and need to fetch each texture pixel continuously during the rendering process. If the same texture is used repetitively, it is not necessary to fetch texture from memory again. Built-in texture cache could significantly improve texture-mapping performance.
With built-in texture cache, each time when a texture miss happens, a segment of texture will be read from texture buffer and stored in an internal texture cache line. In Volari™ V3XE GPU, texture cache is implemented with 8 texel read ports. Therefore the Volari™ V3XE GPU could provide one 8-tap texture filtering pixel rendering per cycle or one dual-texture 4-tap texture filtering pixel rendering per cycle. Under Direct3D benchmark estimation, more than 98%-hit rate has been measured with 8-tap texture filtering mapping. The texture buffer could be located in video memory or AGP system memory. Volari™ V3XE GPU was also optimized for AGP texture buffer.

## 2.7 Digital Video Interface

Volari™ V3XE integrates two 165 MHz high-speed digital, dual data rate video interface with the capability of independently displaying the video data for DVI (digital video interface), TV or VGA monitor. The signal voltage could be 1.8V or 3.3V. The output signal formats include RGB888 and dithered RGB666 video format. SiS301 video encoder supports NTSC and PAL standards and integrates video DACs, anti-flicker circuits, composite video and S video sense circuits. The 301 also supports RGB format output and scaled TMDS flat panel signals. Independent display of digital video interface could be supported. The secondary CRT could have simultaneous display with primary CRT. It could have independent display with primary CRT by different frame rates, different display buffers and different display color depths. It could have under scan scaling for TV and over scan scaling for LCD display. Also it could have horizontal and vertical position adjustment functions.

The table below illustrates the possible dual display applications.

| Volari™ V3XE GPU Primary CRT | Volari™ V3XE GPU VB channel | Volari™ V3XE GPU VA Channel | Mirror View | Dual View | Independent Frame Rate | Scaling Capability |
|---|---|---|---|---|---|---|
| **CRT1** Std. Mode/Enh. mode | - | | **-** | **-** | **-** | **-** |
| - | **LCD** Std. Mode/Enh. Mode | | **-** | **-** | **-** | **Yes** |
| - | **TV** Std. Mode/Enh. Mode | | **-** | **-** | **-** | **Yes** |
| - | **CRT2** Std. Mode/Enh. Mode | | **-** | **-** | **-** | **-** |
| **CRT1** Std. mode | **LCD** Std. Mode | | **Yes** | **-** | **Yes** | **Yes** |
| **CRT1** Std. mode | **TV** Std. Mode | | **Yes** | **-** | **Yes** | **Yes** |
| **CRT1** Std. mode | **CRT2** Std. Mode | | **Yes** | **-** | **Yes** | **-** |
| **CRT1** Std. mode | **LCD** Enh. Mode | | **-** | **Yes** | **Yes** | **Yes** |
| **CRT1** Std. mode | **TV** Enh. Mode | | **-** | **Yes** | **Yes** | **Yes** |
| **CRT1** Std. Mode | **CRT2** Enh. Mode | | **-** | **Yes** | **Yes** | **-** |
| **CRT1** Enh. Mode | **LCD** Enh. Mode | | **Yes** | **Yes** | **Yes** | **Yes** |
| **CRT1** Enh. Mode | **TV** Enh. Mode | | **Yes** | **Yes** | **Yes** | **Yes** |
| **CRT1** Enh. Mode | **CRT2** Enh. Mode | | **Yes** | **Yes** | **Yes** | **-** |
| **-** | **TV** Std. Mode | **LCD** Std. Mode | **Yes** | **-** | **Yes** | **Yes** |
| **-** | **TV** Enh. Mode | **LCD** Std. Mode | **Yes** | **-** | **Yes** | **Yes** |

Maximum CRT1 mode: 2048x1536@85Hz

Maximum CRT2 mode: 1600x1200@60Hz

Maximum LCD mode: 1600x1200@60Hz

Maximum TV mode: 1024x768@60Hz (NTSC), 1024x768@50Hz (PAL)

## 2.8 MPEG-2 Motion Compensation Decoding

Volari™ V3XE integrates an MPEG video decoder that supports MPEG-2 video standards. Basically, this MPEG video decoder is a MPEG motion compensation decoder that takes about 40% MPEG video decoding computational power and the remainder is done by the CPU. Therefore the scheme applied in Volari™ V3XE GPU is the most economic and efficient approach and retains considerable design flexibility. DVD video standard is under the restraint of the silicon design. Volari™ V3XE design requires minimum silicon area but more significantly reduces CPU loading compared to pure software MPEG video decoding. For the Volari™ V3XE GPU design, audio decoding and syntax parsing are done by the CPU but all of the other video tasks will be done by Volari™ V3XE GPU chip.
For MPEG or AC3 audio decoding, it will count on the computation of CPU or an external MPEG or AC3 audio decoder option.

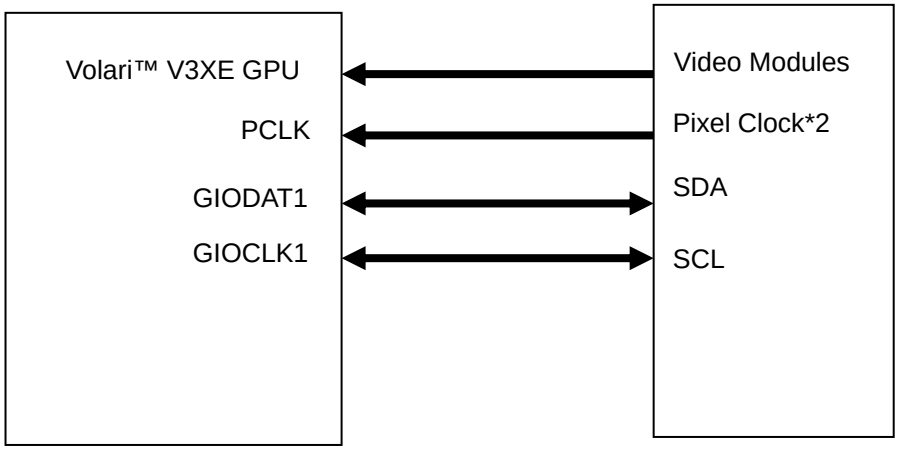
In the process of MPEG video decoding, Volari™ V3XE will allocate four image buffers in off-screen area. These four image buffers are for I-picture, P-picture, B-picture (rendering), and one additional B-picture (displaying). For MPEG-2 decoding, it takes at least 1980K bytes off-screen memory.
To support MPEG-2 video overlay, Volari™ V3XE GPU doubles its video line buffer length and supports up to 1920 pixels width of video playback.

## 2.9 Video Accelerator

Volari™ V3XE GPU video accelerator could work in three different modes: standard FC (feature connector) mode, direct video mode or PCI multimedia mode.
**In standard FC mode,** Volari™ V3XE supports standard VESA™ FC standard.
**In direct video mode,** Volari™ V3XE could work with the several video decoders ex: Conexant BT835 (8-bit SPI mode 1, 2) and CCIR656 video interface format to provide the PC-Video solution. Almost video decoders of all vendors could connect to Volari™ V3XE GPU video interface. After receiving the video data, Volari™ V3XE GPU will perform scaling, cropping and store these video data to the display memory. Furthermore Volari™ V3XE will perform filtering and scaling on the stored video data before overlaying with graphics data for final display.

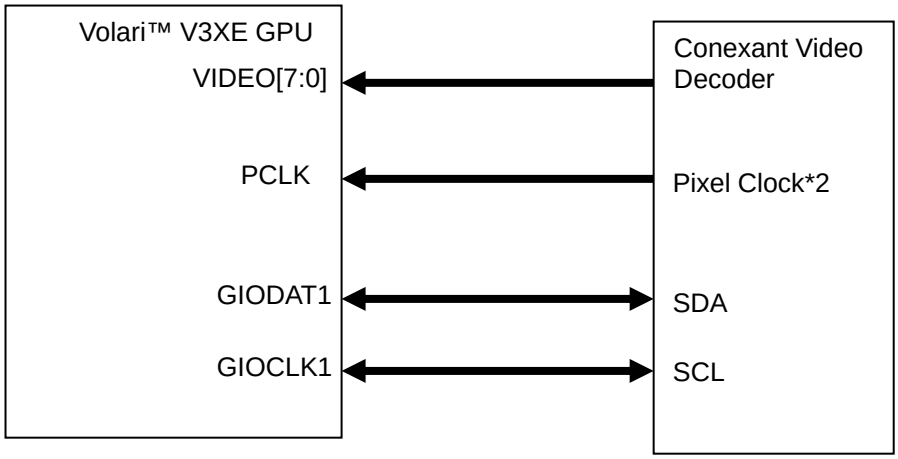
**1. CCIR656 standard mode**

This is a general format supported by almost all video modules. It contains an 8-bit video data port and a clock pin. The synchronization signals are coded into video data stream, so no extra signals are needed.



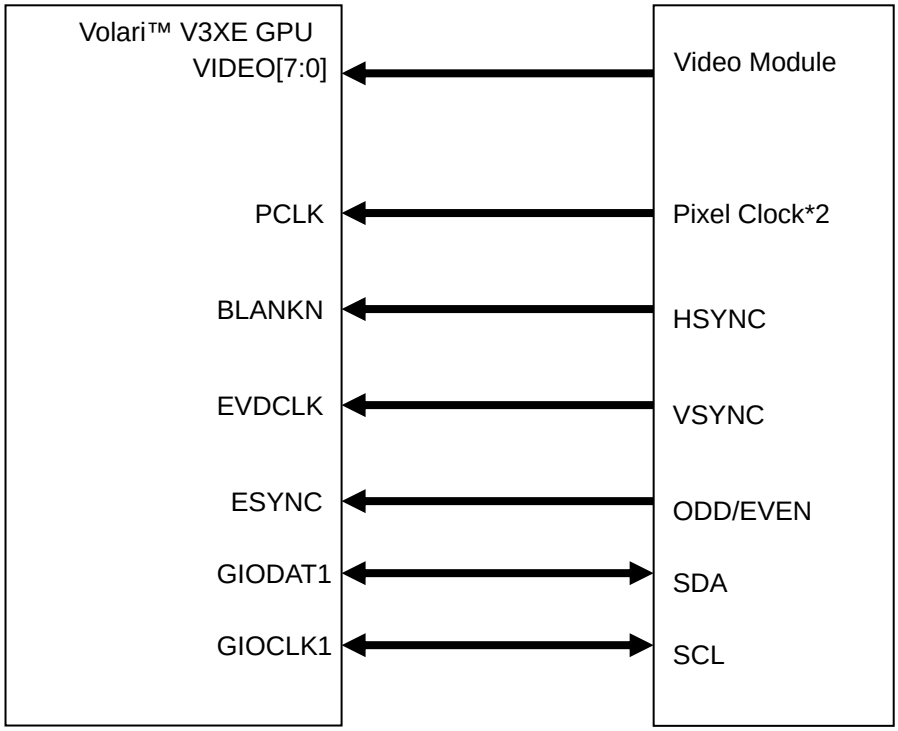

**2. Conexant BT835 compatible (8-bit SPI mode 1, 2)**

This is a special mode supported only by Conexant. It contains an 8-bit video data port and a clock pin, too. The benefit of this mode is that it could support down scaling signal coded inside video data stream.



**3. CCIR601-2 (8-bit YUYV interleave) mode**

This is a format that the video data is not coded and it needs more signals for horizontal synchronous signal, vertical synchronous signal and odd/even signal. It contains an 8-bit video data port, a clock pin, three signal control pins. The data format is 8-bit data stream in sequence of “UYVYUYVY….”.




The video input interface could capture one of RGB565, YUV422 or YUV420 video data format and store the video data into the video frame buffer. The new YUV420 mode could reduce the video capture bandwidth and video capture frame buffer size. The video input unit also provides the horizontal and vertical downscaling filter to generate better video capture quality. The vertical downscaling filter is implemented by a video capture frame buffer read back operation (no line buffer is required).

**In PCI multimedia mode,** Volari™ V3XE GPU supports PCI multimedia design specification to meet with future potential trends.

The Volari™ V3XE GPU could provide one video window overlay with multiple video data formats. The video window could have horizontal and vertical filtering at the same time. The supported video data format includes RGB555, RGB565, YUYV, YVYU, UYVY, VYUY and YUV420 modes. A horizontal downscaling filter is implemented before each video line buffer. It could perform video downscaling filtering. The pre-scaling filter could be 2-tap, 4-tap and 8-tap.

A sub-picture overlaying video stream is implemented with video window for DVD sub-picture display. The sub-picture data is stored in off-screen memory and the sub-picture video data is independent of video data. A 16 entries color palette register is implemented for sub-picture color lookup. A 4-bit blending unit is implemented for combining the video data and the sub-picture data. The scaling factors of sub-picture should be the same with the video window and the sub-picture scaling will match with the playback video.

The video overlay is performed by video color key. The color key could be a range of RGB or YUV formats. If the video data is passed to the color key test, then the video data would be overlaid upon the graphics data.

## 2.10 AGP/PCI Bus Interface

Volari™ V3XE GPU connects directly to the PCI or AGP bus with no glue logic and it decodes the 32-bit address and responds to the applicable control lines. It could execute both of the I/O and memory access as an 8-, 16-, and 32-bit device.
In AGP bus interface, Volari™ V3XE GPU implements full side band or pipeline command features of AGP 4X mode. One 16-stage command FIFO is implemented for reducing the latency time of AGP read access. The AGP interface is used by MPEG commands read, 3D engine texture read, 3D engine vertex data read and all 2D source data read. The AGP of Volari™ V3XE GPU is properly designed to achieve up to 266 MHz AGP 4X clock for maximum 1 GB/sec bandwidth.

## 2.11 BroadBahn™ Memory Architecture

The Display Memory Controller of Volari™ V3XE GPU generates timing for display memory. It could support the following DRAM timing:

- DDR SDRAM

For memory types, it can support 8Mx16, 16Mx16, 4Mx32 and 8Mx32 DDR SDRAM
The maximum frequency of Volari™ V3XE DRAM controller is 200MHz.(DDR) It could support up to 3.2 GB/s bandwidth, with 64-bit DDR SDRAM interface. The DRAM capacity could be up to 128 MB frame buffer size which could support highest bandwidth for texture buffer instead of texture buffer in AGP memory with lower bandwidth. The DRAM controller is pipeline designed: Optimized DRAM arbiter and DDR SDRAM ping-pong bank operation are also implemented to reduce DRAM pre-charge time for achieving the maximum utilization rate of DDR SDRAM. 64-bit external and internal data buses ensure the data throughput meets the maximum 64-bit DDR SDRAM efficiency.

## 2.12 Other Function Blocks

### Attribute Controller

The Attribute Controller formats the display for the screen. Display color selection, text blinking, alternate font selection, and underlining are performed by the Attribute Controller.

### CRT Controller

The CRT Controller generates the HSYNC and VSYNC signals required for the monitor, as well as BLANK signals required by the Attribute Controller.

### CRT FIFO

The CRT FIFO allows the Display Memory Controller to access the display memory for screen refresh at maximum memory speed rather than at the screen refresh rate. It provides hardware auto threshold detection to reach optimum memory utilization rate. When these thresholds are auto detected, the engine wait-time would be reduced to improve overall performance.

### DDC Controller

The DDC Controller provides two different channels to communicate with the monitor which supports DDC level 1 or DDC level 2B. One is DDC CLK channel which is bi-directional and provides the clock for DDC. The other is DDC DATA channel which is bi-directional and could query some information from monitor.

With the advantage of DDC, VGA BIOS could realize the capability of the connected monitor and take adequate action (such as to program the parameters for higher frame rate, ..., etc.) to make end users feel more comfortable.

### Graphics Controller

It performs text manipulation, data rotation, color mapping, and miscellaneous operations.

### Graphics & Video RAMDAC

The RAMDAC contains the color palette and 24-bit true color DAC. The maximum frequency of the RGB DAC is 400 MHz. It could support 2048x1536 video mode.

The color palette, with 256 24-bit entries, converts a color code that specifies the color of a pixel into three 8-bit values, one each for red, green and blue.

The 24-bit true color DAC is designed for direct color graphics mode. It converts each digital color value to three analog voltages for red, green, and blue.

### Read-ahead Cache

With read-ahead cache, the times of the operation of display memory read will be reduced, thus enhance the performance.

### Post Write Buffer

The post write buffer contains a buffer of CPU write accesses to display memory that have not been executed because of memory arbitration. With this buffer, the Volari™ V3XE GPU will release CPU as soon as it records the address and data, and then write into display memory when the display memory is available. Thus CPU performance is increased.

### Internal Triple-Clock Synthesizer

Volari™ V3XE GPU has built-in three clock synthesizers to generate the MCLK, ECLK and DCLK. These clock synthesizers could generate several variable frequencies, thus they could provide the flexibility for selecting the working frequency.

These three clock synthesizers generate MCLK, ECLK and DCLK with single external reference clock (14.318MHz). With this characteristic, we could set the MCLK at the maximum speed that the display memory could work normally, thus it takes the advantage of the real peak memory bandwidth and improves the graphics performance. We could set the ECLK at the maximum speed and the 3D engine could work normally, thus it takes the advantage of the real peak 3D engine bandwidth and improves the graphics performance. The ECLK frequency could be dynamically reduced when the 3D engine is not busy for reducing the whole chip power consumption.

**The following block diagram is for clock synthesizer.**

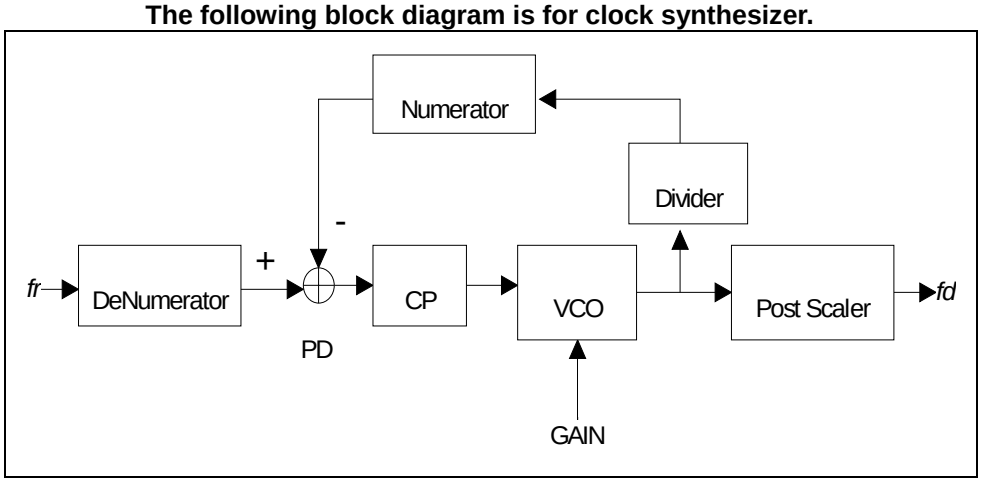



**Figure 2.15 -1 Block Diagram of Clock Synthesizer**

Where PD is phase detection,

CP is charge pump,

VCO is voltage-controlled oscillator,

fr is reference frequency, and

fd is desired frequency.

The operation of clock synthesizer is described as follows:

When the synthesizer outputs the steady frequency, it means that

*fd=fr**((Numerator+1))/(DeNumerator+1))*(Divider/Post Scalar)

With this formula, we could select adequate values for Numerator, DeNumerator, Divider and Post Scalar to obtain the desired frequency.

**Compatibility**

The Volari™ V3XE is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA and Hercules modes.

**Process and Supply Voltages**

Volari™ V3XE is manufactured by 1.5 volts CMOS process. No 5 volts VDD pin is required for the reference of voltage tolerance. The supply voltage for internal logic should be within 1.6 volts ± 5%. The supply voltage for DRAM I/O pads should be within 2.5 volts ± 5% or 3.3 volts ± 5% for DDR. The supply voltage for AGP I/O pads should be within 3.3 volts ± 5% or 1.5 volts ± 5%. The supply voltage for VB interface should be within 1.5 volts ± 5% or 3.3 volts ± 5%. The supply voltage for all analog VDD pins should be within 3.3 volts ± 5%. All other I/O pad supply voltage should be within 3.3 volts ± 5%.

In non-AGP configuration, all the AGP pins must be tight to the ground.

**Software Support**

To fully utilize and support the Volari™ V3XE GPU hardware features, XGI™ Technology has developed a high-performance VESA™ extension compliant BIOS.

Extended graphics and text modes are supported by software application drivers which developed by XGI™ Technology. The following applications are currently supported:

- Microsoft Windows 98/ 98SE[*1]
- Microsoft Windows Me
- Microsoft Windows 2000
- Microsoft Windows XP

[*1]Windows Me drivers could be installed on Windows 98/98SE

Video operation is supported by software application which drivers developed by XGI™ Technology. The following applications are currently supported:

- Microsoft Video For Windows
- Direct Draw driver
- WDM Driver

3D operations are supported by software application drivers developed by XGI™ Technology. The following applications are currently supported:

- Microsoft Direct3D for, Windows 98/ 98SE*, Windows Me, Windows 2000,Windows XP
- OpenGL 1.5[*2] for Windows 98/ 98SE*, Windows Me, Windows 2000 and Windows XP

[*1]Windows Me drivers could be installed on Windows 98/98SE.

[*2] must use Volari reactor driver 1.05.55 later

# 3 Mode Tables

## 3.1 Standard VGA Modes

| MODE | TYPE | DISPLAY SIZE | COLORS SHADES | ALPHA FORMAT | BUFFER START | BOX SIZE | MAX. PAGES |
|---|---|---|---|---|---|---|---|
| 0 | A/N | 320x200 | 16 | 40x25 | B800 | 8x8 | 8 |
| 0* | A/N | 320x350 | 16 | 40x25 | B800 | 8x14 | 8 |
| 0+ | A/N | 360x400 | 16 | 40x25 | B800 | 9x16 | 8 |
| 1 | A/N | 320x200 | 16 | 40x25 | B800 | 8x8 | 8 |
| 1* | A/N | 320x350 | 16 | 40x25 | B800 | 8x14 | 8 |
| 1+ | A/N | 360x400 | 16 | 40x25 | B800 | 9x16 | 8 |
| 2 | A/N | 640x200 | 16 | 80x25 | B800 | 8x8 | 8 |
| 2* | A/N | 640x350 | 16 | 80x25 | B800 | 8x14 | 8 |
| 2+ | A/N | 720x400 | 16 | 80x25 | B800 | 9x16 | 8 |
| 3 | A/N | 640x200 | 16 | 80x25 | B800 | 8x8 | 8 |
| 3* | A/N | 640x350 | 16 | 80x25 | B800 | 8x14 | 8 |
| 3+ | A/N | 720x400 | 16 | 80x25 | B800 | 9x16 | 8 |
| 4 | APA | 320x200 | 4 | 40x25 | B800 | 8x8 | 1 |
| 5 | APA | 320x200 | 4 | 40x25 | B800 | 8x8 | 1 |
| 6 | APA | 640x200 | 2 | 80x25 | B800 | 8x8 | 1 |
| 7 | A/N | 720x350 | 4 | 80x25 | *B000* | 9x14 | 8 |
| 7+ | A/N | 720x400 | 4 | 80x25 | *B000* | 9x16 | 8 |
| 0D | APA | 320x200 | 16 | 40x25 | A000 | 8x8 | 8 |
| 0E | APA | 640x200 | 16 | 80x25 | A000 | 8x8 | 4 |
| 0F | APA | 640x350 | 2 | 80x25 | *B000* | 8x14 | 2 |
| 10 | APA | 640x350 | 16 | 80x25 | A000 | 8x14 | 2 |
| 11 | APA | 640x480 | 2 | 80x30 | A000 | 8x16 | 1 |
| 12 | APA | 640x480 | 16 | 80x30 | A000 | 8x16 | 1 |
| 13 | APA | 320x200 | 256 | 40x25 | A000 | 8x8 | 1 |

Note:1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphics)

| MODE | DISPLAY SIZE | COLORS SHADES | FRAME RATE. | H-SYNC. | VIDEO FREQ. |
|---|---|---|---|---|---|
| 0 | 320x200 | 16 | 70 | 31.5 K | 25.1 M |
| 0* | 320x350 | 16 | 70 | 31.5 K | 25.1 M |
| 0+ | 360x400 | 16 | 70 | 31.5 K | 28.3 M |
| 1 | 320x200 | 16 | 70 | 31.5 K | 25.1 M |
| 1* | 320x350 | 16 | 70 | 31.5 K | 25.1 M |
| 1+ | 360x400 | 16 | 70 | 31.5 K | 28.3 M |
| 2 | 640x200 | 16 | 70 | 31.5 K | 25.1 M |
| 2* | 640x350 | 16 | 70 | 31.5 K | 25.1 M |
| 2+ | 720x400 | 16 | 70 | 31.5 K | 28.3 M |
| 3 | 640x200 | 16 | 70 | 31.5 K | 25.1 M |
| 3* | 640x350 | 16 | 70 | 31.5 K | 25.1 M |
| 3+ | 720x400 | 16 | 70 | 31.5 K | 28.3 M |
| 4 | 320x200 | 4 | 70 | 31.5 K | 25.1 M |
| 5 | 320x200 | 4 | 70 | 31.5 K | 25.1 M |
| 6 | 640x200 | 2 | 70 | 31.5 K | 25.1 M |
| 7* | 720x350 | 4 | 70 | 31.5 K | 28.3 M |
| 7+ | 720x400 | 4 | 70 | 31.5 K | 28.3 M |
| 0D | 320x200 | 16 | 70 | 31.5 K | 25.1 M |
| 0E | 640x200 | 16 | 70 | 31.5 K | 25.1 M |
| 0F | 640x350 | 2 | 70 | 31.5 K | 25.1 M |
| 10 | 640x350 | 16 | 70 | 31.5 K | 25.1 M |
| 11 | 640x480 | 2 | 60 | 31.5 K | 25.1 M |
| 12 | 640x480 | 16 | 60 | 31.5 K | 25.1 M |
| 13 | 320x200 | 256 | 70 | 31.5 K | 25.1 M |

Note:i - interlaced mode

n – Non-interlaced mode

## 3.2 Enhanced video modes

| MODE | TYPE | DISPLAY SIZE | COLORS SHADES | ALPHA FORMAT | BUFFER START | BOX SIZE | MAX. PAGES |
|---|---|---|---|---|---|---|---|
| 6A | APA | 800x600 | 16 | 100x37 | A000 | 8x16 | 1 |
| 2E | APA | 640x480 | 256 | 80x30 | A000 | 8x16 | 1 |
| 2F | APA | 640x400 | 256 | 80x25 | A000 | 8x16 | 1 |
| 30 | APA | 800x600 | 256 | 100x37 | A000 | 8x16 | 1 |
| 5D | APA | 640x400 | 64K | 80x50 | A000 | 8x16 | 1 |
| 38 | APA | 1024x768 | 256 | 128x48 | A000 | 8x16 | 1 |
| 3A | APA | 1280x1024 | 256 | 160x64 | A000 | 8x16 | 1 |
| 3C | APA | 1600x1200 | 256 | 200x75 | A000 | 8x16 | 1 |
| 3D | APA | 1600x1200 | 64K | 200x75 | A000 | 8x16 | 1 |
| 40 | APA | 320x200 | 32K | 40x25 | A000 | 8x8 | 1 |
| 41 | APA | 320x200 | 64K | 40x25 | A000 | 8x8 | 1 |
| 43 | APA | 640x480 | 32K | 80x30 | A000 | 8x16 | 1 |
| 44 | APA | 640x480 | 64K | 80x30 | A000 | 8x16 | 1 |
| 46 | APA | 800x600 | 32K | 100x37 | A000 | 8x16 | 1 |
| 47 | APA | 800x600 | 64K | 100x37 | A000 | 8x16 | 1 |
| 49 | APA | 1024x768 | 32K | 128x48 | A000 | 8x16 | 1 |
| 4A | APA | 1024x768 | 64K | 128x48 | A000 | 8x16 | 1 |
| 4C | APA | 1280x1024 | 32K | 160x64 | A000 | 8x16 | 1 |
| 4D | APA | 1280x1024 | 64K | 160x64 | A000 | 8x16 | 1 |
| 62 | APA | 640x480 | 32bpp | 80x30 | A000 | 8x16 | 1 |
| 63 | APA | 800x600 | 32bpp | 100x37 | A000 | 8x16 | 1 |
| 64 | APA | 1024x768 | 32bpp | 128x48 | A000 | 8x16 | 1 |
| 65 | APA | 1280x1024 | 32bpp | 160x64 | A000 | 8x16 | 1 |
| 66 | APA | 1600x1200 | 32bpp | 200x75 | A000 | 8x16 | 1 |
| 68 | APA | 1920x1440 | 256 | 240x90 | A000 | 8x16 | 1 |
| 69 | APA | 1920x1440 | 64K | 240x90 | A000 | 8x16 | 1 |
| 6B | APA | 1920x1440 | 32bpp | 240x90 | A000 | 8x16 | 1 |
| 6C | APA | 2048*1536 | 256 | 256x96 | A000 | 8x16 | 1 |
| 6D | APA | 2048*1536 | 64K | 256x96 | A000 | 8x16 | 1 |
| 6E | APA | 2048*1536 | 32bpp | 256x96 | A000 | 8x16 | 1 |

Note:APA: All Point Addressable (Graphics)

## For TV mode

| MODE | TYPE | DISPLAY SIZE | COLORS SHADES | ALPHA FORMAT | BUFFER START | BOX SIZE | MAX. PAGES |
|---|---|---|---|---|---|---|---|
| 2E | APA | 640x480 | 256 | 80x30 | A000 | 8x16 | 1 |
| 43 | APA | 640x480 | 32K | 80x30 | A000 | 8x16 | 1 |
| 44 | APA | 640x480 | 64K | 80x30 | A000 | 8x16 | 1 |
| 62 | APA | 640x480 | 32bpp | 80x30 | A000 | 8x16 | 1 |
| 30 | APA | 800x600 | 256 | 100x37 | A000 | 8x16 | 1 |
| 46 | APA | 800x600 | 32K | 100x37 | A000 | 8x16 | 1 |
| 47 | APA | 800x600 | 64K | 100x37 | A000 | 8x16 | 1 |
| 63 | APA | 800x600 | 32bpp | 100x37 | A000 | 8x16 | 1 |
| 38 | APA | 1024x768 | 256 | 128x48 | A000 | 8x16 | 1 |
| 49 | APA | 1024x768 | 32K | 128x48 | A000 | 8x16 | 1 |
| 4A | APA | 1024x768 | 64K | 128x48 | A000 | 8x16 | 1 |
| 64 | APA | 1024x768 | 32bpp | 128x48 | A000 | 8x16 | 1 |
| 3A | APA | 1280x1024 | 256 | 160x64 | A000 | 8x16 | 1 |
| 4C | APA | 1280x1024 | 32K | 160x64 | A000 | 8x16 | 1 |
| 4D | APA | 1280x1024 | 64K | 160x64 | A000 | 8x16 | 1 |
| 65 | APA | 1280x1024 | 32bpp | 160x64 | A000 | 8x16 | 1 |
| 31 | APA | 720X480 | 256 | 90x30 | A000 | 8x16 | 1 |
| 33 | APA | 720X480 | 64k | 90x30 | A000 | 8x16 | 1 |
| 35 | APA | 720X480 | 32BPP | 90x30 | A000 | 8x16 | 1 |
| 32 | APA | 720X576 | 256 | 90x36 | A000 | 8x16 | 1 |
| 34 | APA | 720X576 | 64k | 90x36 | A000 | 8x16 | 1 |
| 36 | APA | 720X576 | 32BPP | 90x36 | A000 | 8x16 | 1 |
| 70 | APA | 800X480 | 256 | 90x30 | A000 | 8x16 | 1 |
| 7A | APA | 800X480 | 64k | 90x30 | A000 | 8x16 | 1 |
| 76 | APA | 800X480 | 32BPP | 90x30 | A000 | 8x16 | 1 |
| 71 | APA | 1024X576 | 256 | 90x36 | A000 | 8x16 | 1 |
| 74 | APA | 1024X576 | 64k | 90x36 | A000 | 8x16 | 1 |
| 77 | APA | 1024X576 | 32BPP | 90x36 | A000 | 8x16 | 1 |
| 79 | APA | 1280X720 | 256 | 90x30 | A000 | 8x16 | 1 |
| 75 | APA | 1280X720 | 64k | 90x30 | A000 | 8x16 | 1 |
| 78 | APA | 1280X720 | 32BPP | 90x30 | A000 | 8x16 | 1 |

| TV Type | 640x480 | 800x600 | 1024x768 | 1280x1024 | 720x480 | 1280x720 | 800x480 | 1024x768 | 1024x576 |
|---|---|---|---|---|---|---|---|---|---|
| PAL | V | V | V | | | | | V | V |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| NTSC | V | V | V | | V | | | V | |
| 525P | V | V | V | | V | | V | V | |
| 750P | V | V | V | | V | V | | V | |
| 1080I | V | V | V | V | | V | V | V | V |

### For LCD mode

| MODE | TYPE | DISPLAY SIZE | COLORS SHADES | ALPHA FORMAT | BUFFER START | BOX SIZE | MAX. PAGES |
|---|---|---|---|---|---|---|---|
| 2E | APA | 640x480 | 256 | 80x30 | A000 | 8x16 | 1 |
| 43 | APA | 640x480 | 32K | 80x30 | A000 | 8x16 | 1 |
| 44 | APA | 640x480 | 64K | 80x30 | A000 | 8x16 | 1 |
| 62 | APA | 640x480 | 32bpp | 80x30 | A000 | 8x16 | 1 |
| 30 | APA | 800x600 | 256 | 100x37 | A000 | 8x16 | 1 |
| 46 | APA | 800x600 | 32K | 100x37 | A000 | 8x16 | 1 |
| 47 | APA | 800x600 | 64K | 100x37 | A000 | 8x16 | 1 |
| 63 | APA | 800x600 | 32bpp | 100x37 | A000 | 8x16 | 1 |
| 38 | APA | 1024x768 | 256 | 128x48 | A000 | 8x16 | 1 |
| 49 | APA | 1024x768 | 32K | 128x48 | A000 | 8x16 | 1 |
| 4A | APA | 1024x768 | 64K | 128x48 | A000 | 8x16 | 1 |
| 64 | APA | 1024x768 | 32bpp | 128x48 | A000 | 8x16 | 1 |
| 3A | APA | 1280x1024 | 256 | 160x64 | A000 | 8x16 | 1 |
| 4C | APA | 1280x1024 | 32K | 160x64 | A000 | 8x16 | 1 |
| 4D | APA | 1280x1024 | 64K | 160x64 | A000 | 8x16 | 1 |
| 65 | APA | 1280x1024 | 32bpp | 160x64 | A000 | 8x16 | 1 |
| 26 | APA | 1400x1050 | 256 | 175x65 | A000 | 8x16 | 1 |
| 27 | APA | 1400x1050 | 64K | 175x65 | A000 | 8x16 | 1 |
| 28 | APA | 1400x1050 | 32bpp | 175x65 | A000 | 8x16 | 1 |
| 3C | APA | 1600x1200 | 256 | 200x75 | A000 | 8x16 | 1 |
| 3D | APA | 1600x1200 | 64K | 200x75 | A000 | 8x16 | 1 |
| 66 | APA | 1600x1200 | 32bpp | 200x75 | A000 | 8x16 | 1 |

## Frequency of enhanced video mode

| MODE | DISPLAY SIZE | COLORS SHADES | FRAME RATE. (Hz) | H-SYNC. (Hz) | VIDEO FREQ. (Hz) |
|---|---|---|---|---|---|
| 25 | 640x480 | 16 | 60 | 31.5 K | 25.1 M |
| 6A | 800x600 | 16 | 56 | 35.1 K | 30.0 M |
| 2E | 640x480 | 256 | 60 | 31.5 K | 25.1 M |
| 2E* | 640x480 | 256 | 72 | 37.9 K | 31.5 M |
| 2E+ | 640x480 | 256 | 75 | 37.5 K | 31.5 M |
| 2E++ | 640x480 | 256 | 85 | 43.4 K | 36.0 M |
| 2F | 640x400 | 256 | 70 | 31.5 K | 25.1 M |
| 30 | 800x600 | 256 | 56 | 35.1 K | 36.0 M |
| 30* | 800x600 | 256 | 60 | 37.9 K | 40.0 M |
| 30+ | 800x600 | 256 | 72 | 48.0 K | 50.0 M |
| 30# | 800x600 | 256 | 75 | 46.8 K | 50.0 M |
| 30## | 800x600 | 256 | 85 | 53.7 K | 56.3 M |
| 5D | 640x400 | 64K | 70 | 31.5 K | 25.1 M |
| 38i | 1024x768 | 256 | 87 | 35.5 K | 44.9 M |
| 38n | 1024x768 | 256 | 60 | 48.4 K | 65.0 M |
| 38n+ | 1024x768 | 256 | 70 | 56.5 K | 75.0 M |
| 38n# | 1024x768 | 256 | 75 | 60.2 K | 80.0 M |
| 38n## | 1024x768 | 256 | 85 | 68.7 K | 94.5 M |
| 3Ai | 1280x1024 | 256 | 87 | 48.8 K | 80.0 M |
| 3An | 1280x1024 | 256 | 60 | 65.0 K | 110.0 M |
| 3An+ | 1280x1024 | 256 | 75 | 80.0 K | 135.0 M |
| 3Cn | 1600x1200 | 256 | 60 | 75.6 K | 135.0 M |
| 3Dn | 1600x1200 | 64K | 60 | 75.6 K | 135.0 M |
| 3Ci | 1600x1200 | 256 | 87 | 75.6 K | 135.0 M |
| 3Cn | 1600x1200 | 256 | 60 | 75.6 K | 135.0 M |
| 3Cn+ | 1600x1200 | 256 | 65 | 75.0 K | 162.0 M |
| 3Cn# | 1600x1200 | 256 | 75 | 81.3 K | 175.5 M |
| 3Cn## | 1600x1200 | 256 | 85 | 93.8 K | 202.5M |

| | | | | | |
|---|---|---|---|---|---|
| 3Di | 1600x1200 | 64K | 87 | 75.6 K | 135.0 M |
| 3Dn | 1600x1200 | 64K | 60 | 75.6 K | 135.0 M |
| 3Dn+ | 1600x1200 | 64K | 65 | 75.0 K | 162.0 M |
| 3Dn# | 1600x1200 | 64K | 75 | 81.3 K | 175.5 M |
| 3Dn## | 1600x1200 | 64K | 85 | 93.8 K | 202.5M |
| 40 | 320x200 | 32K | 70 | 31.5 K | 25.1 M |
| 41 | 320x200 | 64K | 70 | 31.5 K | 25.1 M |
| 42 | 320x200 | 16.8M | 70 | 31.5 K | 25.1 M |
| 43 | 640x480 | 32K | 60 | 31.5 K | 25.1 M |
| 43* | 640x480 | 32K | 72 | 37.9 K | 31.5 M |
| 43+ | 640x480 | 32K | 75 | 37.5 K | 31.5 M |
| 43++ | 640x480 | 32K | 85 | 43.4 K | 36.0 M |
| 44 | 640x480 | 64K | 60 | 31.5 K | 25.1 M |
| 44* | 640x480 | 64K | 72 | 37.9 K | 31.5 M |
| 44+ | 640x480 | 64K | 75 | 37.5 K | 31.5 M |
| 44++ | 640x480 | 64K | 85 | 43.4 K | 36.0 M |
| 46 | 800x600 | 32K | 56 | 35.1 K | 36.0 M |
| 46* | 800x600 | 32K | 60 | 37.9 K | 40.0 M |
| 46+ | 800x600 | 32K | 72 | 48.0 K | 50.0 M |
| 46# | 800x600 | 32K | 75 | 46.8 K | 50.0 M |
| 46## | 800x600 | 32K | 85 | 53.7 K | 56.3 M |
| 47 | 800x600 | 64K | 56 | 35.1 K | 36.0 M |
| 47* | 800x600 | 64K | 60 | 37.9 K | 40.0 M |
| 47+ | 800x600 | 64K | 72 | 48.0 K | 50.0 M |
| 47# | 800x600 | 64K | 75 | 46.8 K | 50.0 M |
| 47## | 800x600 | 64K | 85 | 53.7 K | 56.3 M |
| 49i | 1024x768 | 32K | 87 | 35.5 K | 44.9 M |
| 49n | 1024x768 | 32K | 60 | 48.4 K | 65.0 M |
| 49n+ | 1024x768 | 32K | 70 | 56.5 K | 75.0 M |
| 49n# | 1024x768 | 32K | 75 | 60.0 K | 78.75 M |
| 49n## | 1024x768 | 32K | 85 | 68.7 K | 94.5 M |
| 4Ai | 1024x768 | 64K | 87 | 35.5 K | 44.9 M |
| 4An | 1024x768 | 64K | 60 | 48.4 K | 65.0 M |
| 4An+ | 1024x768 | 64K | 70 | 56.5 K | 75.0 M |

| | | | | | |
|---|---|---|---|---|---|
| 4An# | 1024x768 | 64K | 75 | 60.0 K | 78.75 M |
| 4An## | 1024x768 | 64K | 85 | 68.7 K | 94.5 M |
| 4Ci | 1280x1024 | 32K | 89 | 48.8 K | 80.0 M |
| 4Cn | 1280x1024 | 32K | 60 | 64.0 K | 108.0 M |
| 4Cn# | 1280x1024 | 32K | 75 | 80.0 K | 135.0 M |
| 4Cn## | 1280x1024 | 32K | 85 | 91.1K | 157.5M |
| 4Di | 1280x1024 | 64K | 89 | 48.8 K | 80.0 M |
| 4Dn | 1280x1024 | 64K | 60 | 64.0 K | 108.0 M |
| 4Dn# | 1280x1024 | 64K | 75 | 80.0 K | 135.0 M |
| 4Dn## | 1280x1024 | 64K | 85 | 91.1K | 157.5M |
| 62 | 640x480 | 32BPP | 60 | 31.5 K | 25.1 M |
| 62* | 640x480 | 32BPP | 72 | 37.9 K | 31.5 M |
| 62+ | 640x480 | 32BPP | 75 | 37.5 K | 31.5 M |
| 62++ | 640x480 | 32BPP | 85 | 43.4 K | 36.0 M |
| 63 | 800x600 | 32BPP | 56 | 35.1 K | 36.0 M |
| 63* | 800x600 | 32BPP | 60 | 37.9 K | 40.0 M |
| 63+ | 800x600 | 32BPP | 72 | 48.0 K | 50.0 M |
| 63# | 800x600 | 32BPP | 75 | 46.8 K | 50.0 M |
| 63## | 800x600 | 32BPP | 85 | 53.7 K | 56.3 M |
| 64i | 1024x768 | 32BPP | 87 | 35.5 K | 44.9 M |
| 64n | 1024x768 | 32BPP | 60 | 48.4 K | 65.0 M |
| 64n+ | 1024x768 | 32BPP | 70 | 56.5 K | 75.0 M |
| 64n# | 1024x768 | 32BPP | 75 | 60.0 K | 78.75 M |
| 64n## | 1024x768 | 32BPP | 85 | 68.7 K | 94.5 M |
| 65i | 1280x1024 | 32BPP | 89 | 48.8 K | 80.0 M |
| 65n | 1280x1024 | 32BPP | 60 | 64.0 K | 108.0 M |
| 65n# | 1280x1024 | 32BPP | 75 | 80.0 K | 135.0 M |
| 65n## | 1280x1024 | 32BPP | 85 | 91.1K | 157.5M |
| 66i | 1600x1200 | 32BPP | 87 | 75.6 K | 135.0 M |
| 66n | 1600x1200 | 32BPP | 60 | 75.0 K | 162.0 M |
| 66n+ | 1600x1200 | 32BPP | 65 | 81.3 K | 175.5 M |
| 66n# | 1600x1200 | 32BPP | 75 | 93.8 K | 202.5M |
| 66n## | 1600x1200 | 32BPP | 85 | 106.3 K | 229.5M |
| 68n | 1920x1440 | 256 | 60 | 90.0 K | 234.0M |

| | | | | | |
|---|---|---|---|---|---|
| 68n# | 1920x1440 | 256 | 75 | 112.5 K | 297.0M |
| 68n## | 1920x1440 | 256 | 85 | 127.5 K | 329.0M |
| 69n | 1920X1440 | 64K | 60 | 90.0 K | 234.0M |
| 69n# | 1920X1440 | 64K | 75 | 112.5 K | 297.0M |
| 69n## | 1920x1440 | 64K | 85 | 127.5 K | 329.0M |
| 6Bn | 1920x1440 | 32BPP | 60 | 90.0 K | 234.0M |
| 6Bn# | 1920X1440 | 32BPP | 75 | 112.5 K | 297.0M |
| 6Bn## | 1920X1440 | 32BPP | 85 | 127.5 K | 329.0M |
| 6Cn | 2048x1536 | 256 | 60 | 96.0 K | 264.0M |
| 6Cn# | 2048x1536 | 256 | 75 | 120.0 K | 330.0M |
| 6Cn## | 2048x1536 | 256 | 85 | 136.0 K | 375.0M |
| 6Dn | 2048x1536 | 64K | 60 | 96.0 K | 264.0M |
| 6Dn# | 2048x1536 | 64K | 75 | 120.0 K | 330.0M |
| 6Dn## | 2048x1536 | 64K | 85 | 136.0 K | 375.0M |
| 6En | 2048x1536 | 32BPP | 60 | 96.0 K | 264.0M |
| 6En# | 2048x1536 | 32BPP | 75 | 120.0 K | 330.0M |
| 6En## | 2048x1536 | 32BPP | 85 | 136.0 K | 375.0M |

Note:i - interlaced mode

n – Non-interlaced mode

TV PAL uses FRAME RATE. 50 (Hz), others use FRAME RATE. 60 (Hz)

LCD use FRAME RATE. 60 (Hz)

### 3.3 Low Resolution Modes

| MODE | TYPE | DISPLAY SIZE | COLORS SHADES | ALPHA FORMAT | BUFFER START | BOX SIZE | MAX. PAGES |
|---|---|---|---|---|---|---|---|
| 50 | APA | 320x240 | 256 | 40x30 | A000 | 8x8 | 1 |
| 53 | APA | 320x240 | 32K | 40x30 | A000 | 8x8 | 1 |
| 56 | APA | 320x240 | 64K | 40x30 | A000 | 8x8 | 1 |
| 51 | APA | 400x330 | 256 | 50x38 | A000 | 8x8 | 1 |
| 54 | APA | 400x330 | 32K | 50x38 | A000 | 8x8 | 1 |
| 57 | APA | 400x330 | 64K | 50x38 | A000 | 8x8 | 1 |
| 52 | APA | 512x384 | 256 | 64x48 | A000 | 8x8 | 1 |
| 55 | APA | 512x384 | 32K | 64x48 | A000 | 8x8 | 1 |
| 58 | APA | 512x384 | 64K | 64x48 | A000 | 8x8 | 1 |

Note:1. A/N: Alpha/Numeric

2. APA: All Point Addressable (Graphics)

## 3.4 Supported Enhanced CRT Mode and Memory Configuration Table (MCLK=200MHz)

| MODE | DCLK (HZ) | PAGE SIZE (BYTE) | BAND WIDTH (BYTE/S) | VIDEO OVERLAY | DRAM REQUIREMENT (BYTE) | DDR |
|---|---|---|---|---|---|---|
| 640x480x8@60NI | 25.1M | 330K | 25M | Yes | 4M | Yes |
| 640x480x16@60NI | 25.1M | 600K | 50M | Yes | 4M | Yes |
| 640x480x32@60NI | 25.1M | 1.2M | 100M | Yes | 4M | Yes |
| 640x480x8@72NI | 31.5M | 330K | 31.5M | Yes | 4M | Yes |
| 640x480x16@72NI | 31.5M | 600K | 63M | Yes | 4M | Yes |
| 640x480x32@72NI | 31.5M | 1.2M | 126M | Yes | 4M | Yes |
| 640x480x8@75NI | 31.5M | 330K | 31.5M | Yes | 4M | Yes |
| 640x480x16@75NI | 31.5M | 600K | 63M | Yes | 4M | Yes |
| 640x480x32@75NI | 31.5M | 1.2M | 126M | Yes | 4M | Yes |
| 640x480x8@85NI | 36M | 330K | 36M | Yes | 4M | Yes |
| 640x480x16@85NI | 36M | 600K | 72M | Yes | 4M | Yes |
| 640x480x32@85NI | 36M | 1.2M | 144M | Yes | 4M | Yes |
| 640x480x8@120NI | 56M | 330K | 56M | Yes | 4M | Yes |
| 640x480x16@120NI | 56M | 600K | 112M | Yes | 4M | Yes |
| 640x480x32@120NI | 56M | 1.2M | 224M | Yes | 4M | Yes |
| 800x600x8@60NI | 40M | 468K | 40M | Yes | 4M | Yes |
| 800x600x16@60NI | 40M | 938K | 80M | Yes | 4M | Yes |
| 800x600x32@60NI | 40M | 1.857M | 160M | Yes | 4M | Yes |
| 800x600x8@72NI | 50M | 468K | 50M | Yes | 4M | Yes |
| 800x600x16@72NI | 50M | 938K | 100M | Yes | 4M | Yes |
| 800x600x32@72NI | 50M | 1.857M | 200M | Yes | 4M | Yes |
| 800x600x8@75NI | 50M | 468K | 50M | Yes | 4M | Yes |
| 800x600x16@75NI | 50M | 938K | 100M | Yes | 4M | Yes |
| 800x600x32@75NI | 50M | 1.857M | 200M | Yes | 4M | Yes |
| 800x600x8@85NI | 56.3M | 468K | 56.3M | Yes | 4M | Yes |
| 800x600x16@85NI | 56.3M | 938K | 112.6M | Yes | 4M | Yes |
| 800x600x32@85NI | 56.3M | 1.857M | 225.2M | Yes | 4M | Yes |
| 800x600x8@120NI | 80M | 468K | 80M | Yes | 4M | Yes |
| 800x600x16@120NI | 80M | 938K | 160M | Yes | 4M | Yes |
| 800x600x32@120NI | 80M | 1.857M | 320M | Yes | 4M | Yes |
| 800x600x8@160NI | 108M | 468K | 108M | Yes | 4M | Yes |
| 800x600x16@160NI | 108M | 938K | 216M | Yes | 4M | Yes |

| | | | | | | |
|---|---|---|---|---|---|---|
| 800x600x32@160NI | 108M | 1.857M | 432M | Yes | 4M | Yes |
| 1024x768x8@60NI | 65M | 0.768M | 65M | Yes | 4M | Yes |
| 1024x768x16@60NI | 65M | 1.536M | 130M | Yes | 4M | Yes |
| 1024x768x32@60NI | 65M | 3.072M | 260M | Yes | 4M | Yes |
| 1024x768x8@75NI | 78.75M | 0.768M | 78.75M | Yes | 4M | Yes |
| 1024x768x16@75NI | 78.75M | 1.536M | 157.5M | Yes | 4M | Yes |
| 1024x768x32@75NI | 78.75M | 3.072M | 330M | Yes | 4M | Yes |
| 1024x768x8@85NI | 94.5M | 0.768M | 94.5M | Yes | 4M | Yes |
| 1024x768x16@85NI | 94.5M | 1.536M | 189M | Yes | 4M | Yes |
| 1024x768x32@85NI | 94.5M | 3.072M | 398M | Yes | 4M | Yes |
| 1024x768x8@120NI | 132M | 0.768M | 132M | Yes | 4M | Yes |
| 1024x768x16@120NI | 132M | 1.536M | 264M | Yes | 4M | Yes |
| 1024x768x32@120NI | 132M | 3.072M | 528M | Yes | 4M | Yes |
| 1024x768x8@160NI | 177M | 0.768M | 177M | Yes | 4M | Yes |
| 1024x768x16@160NI | 177M | 1.536M | 354M | Yes | 4M | Yes |
| 1024x768x32@160NI | 177M | 3.072M | 531M | Yes | 4M | Yes |
| 1152x864x8@60 | 83.6M | 972K | 83.6M | Yes | 4M | Yes |
| 1152x864x16@60 | 83.6M | 1.944M | 167.2M | Yes | 4M | Yes |
| 1152x864x32@60 | 83.6M | 3.888M | 334.4M | Yes | 4M | Yes |
| 1152x864x8@75 | 104.5M | 972K | 104.5M | Yes | 4M | Yes |
| 1152x864x16@75 | 104.5M | 1.944M | 209M | Yes | 4M | Yes |
| 1152x864x32@75 | 104.5M | 3.888M | 418M | Yes | 4M | Yes |
| 1280x960x8@60 | 103.2M | 1.2M | 103.2M | Yes | 4M | Yes |
| 1280x960x16@60 | 103.2M | 2.4M | 206.4M | Yes | 4M | Yes |
| 1280x960x32@60 | 103.2M | 4.8M | 512.8M | Yes | 4M | Yes |
| 1280x960x8@75 | 129.02M | 1.2M | 129.02M | Yes | 4M | Yes |
| 1280x960x16@75 | 129.02M | 2.4M | 258.04M | Yes | 4M | Yes |
| 1280x960x32@75 | 129.02M | 4.8M | 516.08M | Yes | 8M | Yes |
| 1280x960x8@85 | 146.22M | 1.2M | 146.22M | Yes | 4M | Yes |
| 1280x960x16@85 | 146.22M | 2.4M | 292.44M | Yes | 4M | Yes |
| 1280x960x32@85 | 146.22M | 4.8M | 584.88M | Yes | 8M | Yes |
| 1280x960x8@120 | 206.43M | 1.2M | 206.43M | Yes | 4M | Yes |
| 1280x960x16@120 | 206.43M | 2.4M | 412.86M | Yes | 4M | Yes |
| 1280x960x32@120 | 206.43M | 4.8M | 825.72M | Yes | 8M | Yes |
| 1280x960x8@160 | 275.25M | 1.2M | 275.25M | Yes | 4M | Yes |

| | | | | | | |
|---|---|---|---|---|---|---|
| 1280x960x16@160 | 275.25M | 2.4M | 550.50M | Yes | 4M | Yes |
| 1280x960x32@160 | 275.25M | 4.8M | 1101.0M | Yes | 8M | Yes |
| 1280x1024x8@60NI | 110M | 1.28M | 110M | Yes | 4M | Yes |
| 1280x1024x16@60NI | 110M | 2.56M | 220M | Yes | 4M | Yes |
| 1280x1024x32@60NI | 110M | 5.12M | 440M | Yes | 8M | Yes |
| 1280x1024x8@75NI | 135M | 1.28M | 135M | Yes | 4M | Yes |
| 1280x1024x16@75NI | 135M | 2.56M | 270M | Yes | 4M | Yes |
| 1280x1024x32@75NI | 135M | 5.12M | 540M | Yes | 8M | Yes |
| 1280x1024x8@85NI | 157.5M | 1.28M | 157.5M | Yes | 4M | Yes |
| 1280x1024x16@85NI | 157.5M | 2.56M | 330M | Yes | 4M | Yes |
| 1280x1024x32@85NI | 157.5M | 5.12M | 630M | Yes | 8M | Yes |
| 1280x1024x8@120NI | 220M | 1.28M | 157.5M | No | 4M | Yes |
| 1280x1024x16@120NI | 220M | 2.56M | 330M | No | 4M | Yes |
| 1280x1024x32@120NI | 220M | 5.12M | 630M | No | 8M | Yes |
| 1280x1024x8@160NI | 294M | 1.28M | 294M | No | 4M | Yes |
| 1280x1024x16@160NI | 294M | 2.56M | 588M | No | 4M | Yes |
| 1280x1024x32@160NI | 294M | 5.12M | 882M | No | 8M | Yes |
| 1600x1200x8@60NI | 162M | 1.875M | 162M | Yes | 4M | Yes |
| 1600x1200x16@60NI | 162M | 3.75M | 324M | Yes | 4M | Yes |
| 1600x1200x32@60NI | 162M | 7.5M | 648M | Yes | 8M | Yes |
| 1600x1200x8@65NI | 176M | 1.875M | 176M | No | 4M | Yes |
| 1600x1200x16@65NI | 176M | 3.75M | 352M | No | 4M | Yes |
| 1600x1200x32@65NI | 176M | 7.5M | 528M | No | 8M | Yes |
| 1600x1200x8@70NI | 190M | 1.875M | 190M | No | 4M | Yes |
| 1600x1200x16@70NI | 190M | 3.75M | 380M | No | 4M | Yes |
| 1600x1200x32@70NI | 190M | 7.5M | 570M | No | 8M | Yes |
| 1600x1200x8@75NI | 202.5M | 1.875M | 202.5M | No | 4M | Yes |
| 1600x1200x16@75NI | 202.5M | 3.75M | 405M | No | 4M | Yes |
| 1600x1200x32@75NI | 202.5M | 7.5M | 910M | No | 8M | Yes |
| 1600x1200x8@85NI | 230M | 1.875M | 230M | No | 4M | Yes |
| 1600x1200x16@85NI | 230M | 3.75M | 460M | No | 4M | Yes |
| 1600x1200x32@85NI | 230M | 7.5M | 920M | No | 8M | Yes |
| 1600x1200x8@120NI | 270M | 1.875M | 270M | No | 4M | Yes |
| 1600x1200x16@120NI | 270M | 3.75M | 540M | No | 4M | Yes |
| 1600x1200x32@120NI | 270M | 7.5M | 1.08G | No | 8M | Yes |

| | | | | | | |
|---|---|---|---|---|---|---|
| 1920x1440x8@60NI | 234M | 2.76M | 234M | No | 4M | Yes |
| 1920x1440x16@60NI | 234M | 5.53M | 468M | No | 8M | Yes |
| 1920x1440x32@60NI | 234M | 11.6M | 936M | No | 16M | Yes |
| 1920x1440x8@65NI | 255M | 2.76M | 255M | No | 4M | Yes |
| 1920x1440x16@65NI | 255M | 5.53M | 510M | No | 8M | Yes |
| 1920x1440x32@65NI | 255M | 11.6M | 765M | No | 16M | Yes |
| 1920x1440x8@70NI | 275M | 2.76M | 275M | No | 4M | Yes |
| 1920x1440x16@70NI | 275M | 5.53M | 550M | No | 8M | Yes |
| 1920x1440x32@70NI | 275M | 11.6M | 825M | No | 16M | Yes |
| 1920x1440x8@75NI | 297M | 2.76M | 297M | No | 4M | Yes |
| 1920x1440x16@75NI | 297M | 5.53M | 594M | No | 8M | Yes |
| 1920x1440x32@75NI | 297M | 11.6M | 1.19G | No | 16M | Yes |
| 1920x1440x8@85NI | 329M | 2.76M | 329M | No | 4M | Yes |
| 1920x1440x16@85NI | 329M | 5.53M | 658M | No | 8M | Yes |
| 1920x1440x32@85NI | 329M | 11.6M | 1.32G | No | 16M | Yes |
| 2048x1536x8@60NI | 264M | 3.0M | 264M | No | 4M | Yes |
| 2048x1536x16@60NI | 264M | 6.0M | 528M | No | 8M | Yes |
| 2048x1536x32@60NI | 264M | 12.0M | 1.06G | No | 16M | Yes |
| 2048x1536x8@65NI | 290M | 3.0M | 290M | No | 4M | Yes |
| 2048x1536x16@65NI | 290M | 6.0M | 580M | No | 8M | Yes |
| 2048x1536x32@65NI | 290M | 12.0M | 870M | No | 16M | Yes |
| 2048x1536x8@70NI | 310M | 3.0M | 310M | No | 4M | Yes |
| 2048x1536x16@70NI | 310M | 6.0M | 620M | No | 8M | Yes |
| 2048x1536x32@70NI | 310M | 12.0M | 930M | No | 16M | Yes |
| 2048x1536x8@75NI | 330M | 3.0M | 330M | No | 4M | Yes |
| 2048x1536x16@75NI | 330M | 6.0M | 660M | No | 8M | Yes |
| 2048x1536x32@75NI | 330M | 12.0M | 1.32G | No | 16M | Yes |
| 2048x1536x8@85NI | 375M | 3.0M | 375M | No | 4M | Yes |
| 2048x1536x16@85NI | 375M | 6.0M | 750M | No | 8M | Yes |
| 2048x1536x32@85NI | 375M | 12.0M | 1.5G | No | 16M | Yes |

# 4 Volari™ V3XE Pin List and Assignment

**AGP/PCI Bus total 74 balls**

| Ball location | Signal name | Type | Description |
|---|---|---|---|
| A6 | RSTN | I | PCI Reset is used to bring PCI-specific registers, sequencer, and signals to a consistent state. This pin has 5V tolerance. |
| A5 | CLK | I | PCI Bus Clock provides timing for all transactions on PCI bus. This pin has 5V tolerance. |
| B6 | INTAN | O | PCI Interrupt indicates the interrupt signal generated by Volari™ V3XE GPU. This pin has 5V tolerance. |
| B5 | MBDET | I | AGP3.0 motherboard detect pin. It should be short to VSS by AGP3.0 motherboard. This pin is 5V tolerance. |
| * | AD[31:0] | I/O | PCI Address/Data Bus is multiplexed on the same pins. The address phase is the clock cycle in which FRAMEN is asserted and the data phase is immediately after the address phase. |
| V6<br>R1<br>M2<br>L5 | CBE0N<br>CBE1N<br>CBE2N<br>CBE3N | I/O | PCI Command/Byte Enable Bus is multiplexed on the same pins. During the address phase of a transaction, C/BE define the bus command, and during the data phase C/BE are used as Byte Enable. |
| T5 | PAR | I/O | PCI Parity Bit is even parity across AD[31..0] and CBE[3..0]N. |
| N6 | FRAMEN | I/O | PCI Frame Cycle is driven by the current master to indicate the beginning and duration of an access. |
| R4 | TRDYN | I/O | PCI Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. |
| P1 | IRDYN | I/O | PCI Initiator ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. |
| R6 | STOPN | I/O | PCI Stop indicates the current target is requesting the master to stop the current transaction. |
| P2 | DEVSELN | I/O | PCI Device Select indicates whether any device on the bus has been selected. |
| C5 | GNTN | I | PCI Master Grant indicates to the agent that access to the bus has been granted. |
| A2 | REQN | O | Used to request access to the bus to initiate a PCI or an AGP Request. |
| B3,<br>B4, B1 | ST0,<br>ST1, ST2 | I | AGP Status bus provides information from the arbiter to Master on what it may do. |
| D3 | RBFN | O | AGP Read Buffer Full indicates if the master is ready to accept previously requested low priority read data or not. |
| F6 | WBFN/<br>IDSEL | I/O | PCI Initialization Device Select is used as a chip selected during Configuration Read and Write transactions. |
| W4<br>K3 | ADSTBF0<br>ADSTBF1 | I/O | AGP AD Bus Strobe[0..1] provide timing for 2X data transfer mode on the AD[31..0]. |
| W5<br>K4 | ADSTBS0<br>ADSTBS1 | I/O | AGP AD Bus Strobe [0..1]# provide timing for 4X/8X data transfer mode on AD[31..0]. |
| F3 | SBSTBF | O | AGP Side Band Strobe provides timing for SBA[0..7] and is always driven by the AGP master. |
| F4 | SBSTBS | O | AGP Side Band Strobe# provides timing for SBA [0..7] when 4X/8X timing is supported and is always driven by the AGP master. |
| G5,G1,G6,G3<br>F5,E1,D4,E2 | SBA[7:0] | O | Side Band Address port provides an additional bus to pass requests to the target from the master |
| C4 | DBIHI<br>/<br>PIPE | I/O | (AGP3.0 only) This is a bit that goes along with AD[31:16] to indicate whether AD[31:16] needs to be inverted on the receiving end.<br>(AGP2.0/AGP1.0 only) Pipelined request is asserted by the current master to indicate a full width request is to be enquired by the target. |

| | | | |
|---|---|---|---|
| D1 | DBILO | I/O | (AGP3.0 only) This is a bit that goes along with AD[15:0] to indicate whether AD[15:0] needs to be inverted on the receiving end. |
| T2 | AGPVREF33 | AI | AGP 3.3v reference voltage for AD[31..0] and AD_STBF[1:0] I/O pads. |
| M8, T8 | AGPVREFCG | AI | AGP 1.5v or 0.8v reference voltage for AD[31..0] and ADSTBF[1:0], ADSTBS[1:0] I/O pads. |
| N3 | AGPVOHREF | AI | AGP3.0 output reference voltage |
| N1 | AGPRSET | AI | AGP calibration reference resistor |

**DRAM Channel A Bus total 66 balls**

| Ball location | Signal name | Type | Description |
|---|---|---|---|
| AC30, AC29 | SCLKA, SCLKAN | O | Clock Out to memory |
| T27 | CSA | O | Chip select |
| U25 | WEA | O | Write Enable |
| T26 | RASA | O | Row address strobe |
| U26 | CASA | O | Column address strobe |
| AB29 | CKEA | O | Clock Enable |
| AF28, AD27, AF21, AJ21 | DQMA[3:0] | O | Data Mask enable in write cycle |
| * | MAA[14:0] | O | Memory address bus |
| * | DQA[31:0] | I/O | Data In /Data Out |
| AJ28, AE28, AE21, AK21 | DDRASTB [3:0] | I/O | Bi-directional Data Strobe |
| AA8,AC21 | MVREF | AI | Reference voltage of DDR SST-2 VTT |
| AF18 | MNRSET | AI | DDR NMOS calibration reference resistor |
| AH18 | MPRSET | AI | DDR PMOS calibration reference resistor |

**DRAM Channel B Bus total 62 balls**

| Ball location | Signal name | Type | Description |
|---|---|---|---|
| AJ12, AK11 | SCLKB, SCLKBN | O | Clock Out to memory |
| AF15 | CSB | O | Chip select |
| AG14 | WEB | O | Column address strobe |
| AG15 | RASB | O | Row Address Strobe |
| AE14 | CASB | O | Column Address Strobe |
| AK12 | CKEB | O | Clock Enable |
| AK5, AG8, AB6, AH3 | DQMB[3:0] | O | Data Mask enable in write cycle |
| * | MAB[14:0] | O | Memory address bus |
| * | DQB[31:0] | I/O | Data In /Data Out |
| AJ5, AH10, AC6, AF1 | DDRBSTB [3:0] | I/O | Bi-directional Data Strobe |

**FC VMI Bus total 19 balls**

| Ball location | Signal name | Type | Description |
|---|---|---|---|
| F9 | HSYNC | O | Horizontal sync |
| F10 | VSYNC | O | Vertical sync |
| A29 | PCLK/VDCLK | I/O | Pixel clock/Video input port clock |
| * | VIDEO[7:0] | I/O | Video Data Bus |
| F27 | EVIDEO | I/O | Enable Video Data Input, active low |
| B29 | BLANKN/ VDHSYNC | I/O | Blank Video Signal/Video input port horizontal sync |
| E28 | ESYNC/ VDFIELD | I/O | Enable Sync Input, active low/Video input port field |
| D29 | EVDCLK/ VDVSYNC | I/O | Enable Video Clock Input, active low/Video input port vertical sync |
| F8 | DDCDAT | I/O | Display Data Channel Data line |
| E11 | DDCCLK | I/O | Display Data Channel clock line |
| C30 | GIODAT1 | I/O | General I/O Data bit |
| B30 | GIOCLK1 | I/O | General I/O Clock bit |

**ROM Bus total 28 balls**

| Ball location | Signal name | Type | Description |
|---|---|---|---|
| K28 | ROMCSN/ SPICS | O | ROM chip select/SPI chip select |
| L29 | ROMOEN/ SPISI | I/O | ROM output enable/SPI data in |
| J26 | ROMWEN | I/O | ROM write enable |
| J28 | ROMMA16/ SPICK | I/O | ROM address bus with power on trapping/ SPI clock |
| * | ROMMA[15:0] | I/O | ROM address bus with power on trapping |
| J30 | ROMMD7/SPISO | I/O | ROM data bus with power on trapping/SPI data out |
| * | ROMMD[6:0] | I/O | ROM data bus with power on trapping |

**VB Primary Channel Interface total 17 balls**

| Ball location | Signal name | Type | Description |
|---|---|---|---|
| F25 | VAHSYNC | O | Horizontal sync of VB primary channel |
| E25 | VAVSYNC | O | Vertical sync of VB primary channel |
| A25 | VADE | O | Data valid of VB primary channel |
| C26 | VACLK | I | Clock input from VB primary channel |
| C22 | VAGCLK | O | Clock output to VB primary channel |
| * | VAD[11:0] | O | Primary digit data output channel |

**VB Secondary Interface total 21 balls**

| Ball location | Signal name | Type | Description |
|---|---|---|---|
| C17 | VBHSYNC | O | Horizontal sync of VB secondary channel |
| D17 | VBVSYNC | O | Vertical sync of VB secondary channel |
| A16 | VBDE | O | Data valid of VB secondary channel |
| E17 | VBCLK | I | Clock input from VB secondary channel |
| D19 | VBGCLK | O | Clock output to VB secondary channel |
| B25 | VBCAD | I/O | VB host command, address and data signal |
| A26 | VBHCLK | O | VB host clock output |
| B16, B17 | VBCTL1, VBCTL0 | O | VB control signals |
| * | VBD[11:0] | O | Secondary digit data output channel |

**VGA DAC total 5 balls**

| Ball location | Signal name | Type | Description |
|---|---|---|---|
| A8 | R | A | Red video signal output |
| A9 | G | A | Green video signal output |
| A10 | B | A | Blue video signal output |
| A11 | RSET | A | Reference resistor |
| B10 | COMP | A | Compensation pin |

**Misc. signals total 14 Balls**

| Ball location | Signal name | Type | Description |
|---|---|---|---|
| A12 | REFOSCI | I | Reference clock 14.31818 MHz input |
| B12 | REFOSCO | O | Reference clock 14.31818 MHz output |
| E9 | SPIN | I | Spread spectrum reference clock 14.31818 MHz input |
| F12 | VBRCLK | O | Provide reference clock 14.31818 MHz to 301 |
| A3 | PWRSTN | I | Power on reset of clock generator |
| D8 | ENTEST | I | Test enable |
| D30 | GPIO | I/O | General purpose in/out pin |
| E29 | GPIO2 | I/O | General purpose in/out pin |
| F28 | GPIO3 | I/O | General purpose in/out pin |
| **AE18** | **TDIODE** | **A** | **Thermal Diode** |
| **D9,D10,E10** | **TRAP[2:0]** | **I** | **Reserved(NC)** |
| **A4** | **PSCHIP** | **I** | **Reserved(NC)** |

**Power balls total 455 balls**

| Ball location | Signal name | Type | Description |
|---|---|---|---|
| C13 | AVDDDCLK | P | 3.3V Analog power (DCLK generator) |
| D13 | AVSSDCLK | P | Analog ground (DCLK generator) |
| C14 | AVDDMCLK | P | 3.3V Analog power (MCLK generator) |
| D14 | AVSSMCLK | P | Analog ground (MCLK generator) |
| E14 | AVDDECLK | P | 3.3V Analog power (ECLK generator) |
| F14 | AVSSECLK | P | Analog ground (ECLK generator) |
| D6 | AVDDDLL | P | 3.3V Analog power (BCLK DLL) |
| C6 | AVSSDLL | P | Analog ground (BCLK DLL) |
| B9 | AVDDDAC1 | P | 3.3V Analog power (DAC) |
| C10 | AVDDDAC2 | P | 3.3V Analog power (DAC) |
| B8 | AVSSDAC1 | P | Analog ground (DAC) |
| C11 | AVSSDAC2 | P | Analog ground (DAC) |
| AH19 | AVDDMDLL1 | P | 3.3V Analog power (DDR DLL) |
| AG19 | AVSSMDLL1 | P | Analog ground (DDR DLL) |
| U8,J8 | RVSSQ | P | AGP reference voltage ground |
| * | OVDD3 | P | 3.3V power for FC and ROM |
| * | OVDDQ | P | 1.5V/3.3V for AGP |
| * | OVDDM | P | 1.8V/2.5V for DRAM I/O |
| * | OVDDVB | P | 1.8V/3.3V for VB interface |
| * | PVDD | P | 3.3V for I/O pre-driving |
| * | IVDD | P | 1.6V for core power |
| * | GND | P | Ground |

Note:

P = power pin

I = input pin

O = output pin

I/O = input/output pin

A = analog pin